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Kao et al.

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(54) **TFT SUBSTRATE AND METHOD FOR MAKING SAME**

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(58) **Field of Classification Search**
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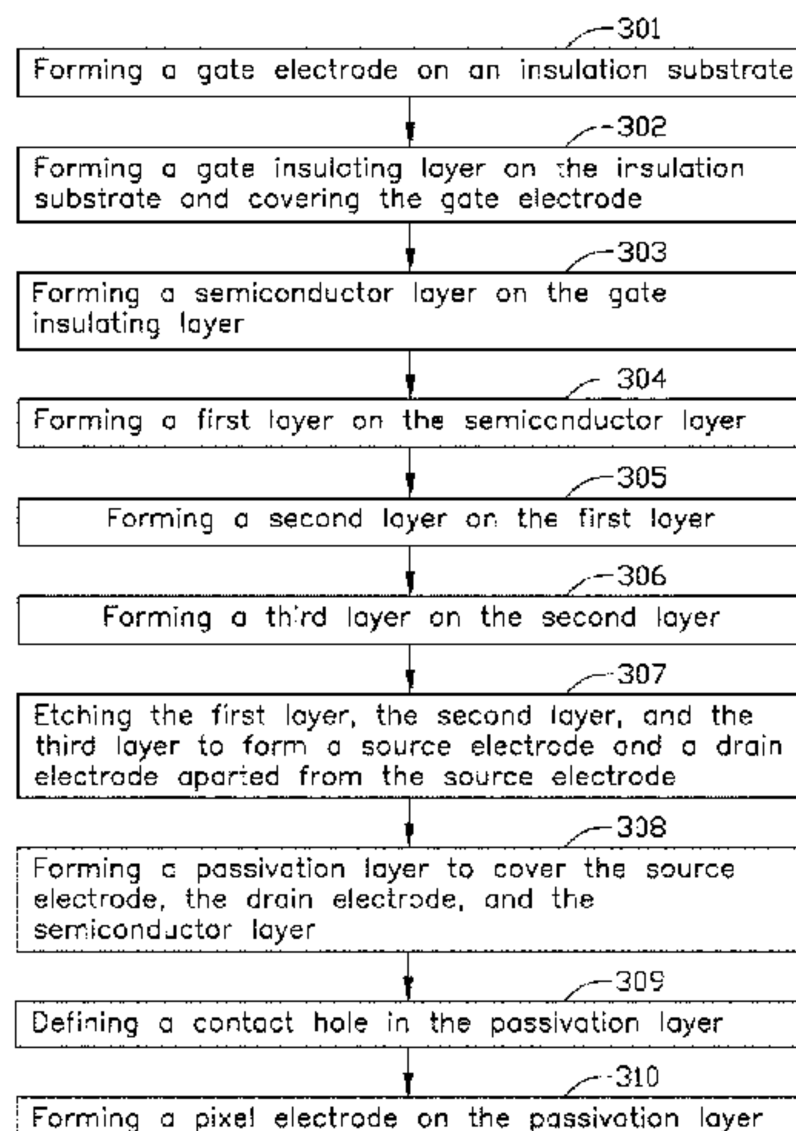
(57) **ABSTRACT**

A high-performance TFT substrate (**100**) for a flat panel display includes a substrate (**110**), a first conductive layer (**130**) on the substrate (**110**), a semiconductor layer (**103**) positioned on the first conductive layer (**130**), and a second conductive layer (**150**) positioned on the semiconductor layer (**103**). The first conductive layer (**130**) defines a gate electrode (**101**). The second conductive layer (**150**) defines a source electrode (**105**) and a drain electrode (**106**) spaced apart from the source electrode (**105**). The second conductive layer (**150**) includes a first layer (**151**) on the semiconductor layer (**103**) and a second layer (**152**) positioned on the
(Continued)



first layer (**151**). The first layer (**151**) can be made of metal oxide. The second layer (**152**) can be made of aluminum or aluminum alloy.

8 Claims, 4 Drawing Sheets

(51) **Int. Cl.**

H01L 27/12	(2006.01)
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H01L 29/24	(2006.01)
H01L 21/465	(2006.01)
H01L 29/04	(2006.01)
H01L 29/417	(2006.01)
H01L 21/28	(2006.01)
H01L 21/768	(2006.01)
H01L 27/32	(2006.01)

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(58) **Field of Classification Search**
CPC H01L 29/66969; H01L 29/78618; H01L 21/02164; H01L 21/0217; H01L 21/02491; H01L 21/02631; H01L 21/465; H01L 27/1222; H01L 27/1225; H01L 27/124; H01L 27/1262; H01L 27/1285; H01L 21/28; H01L 21/76846
See application file for complete search history.

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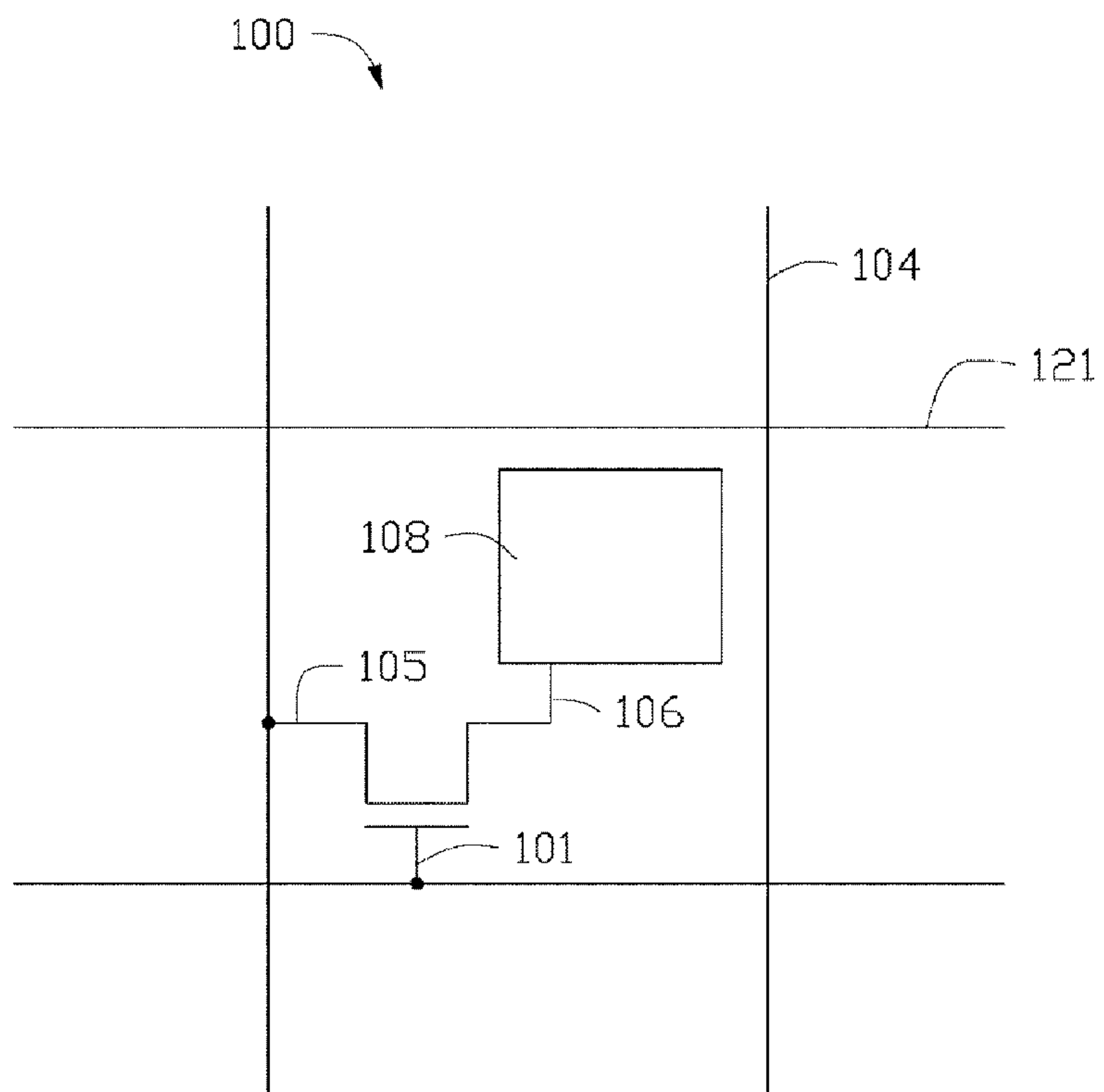
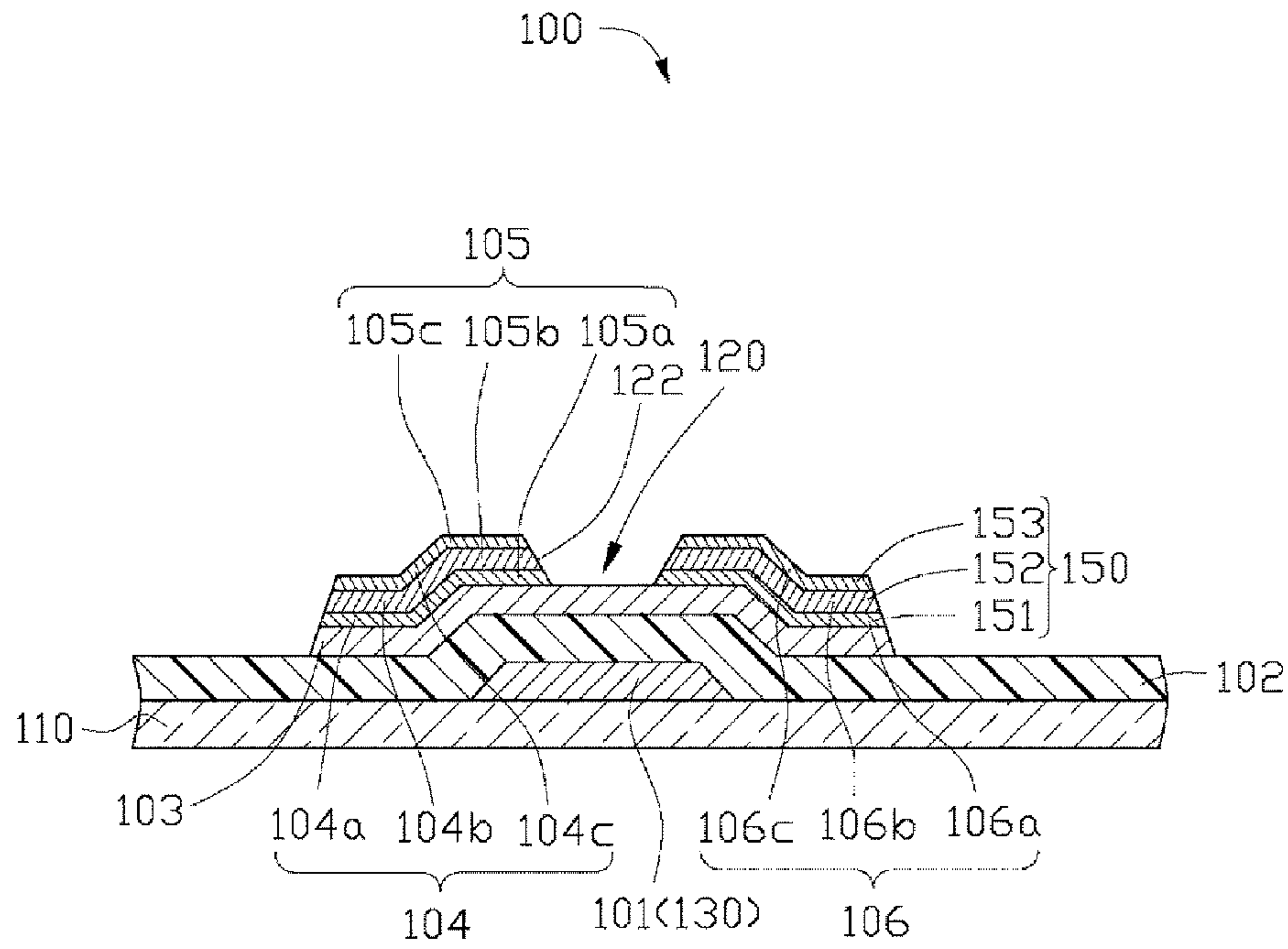
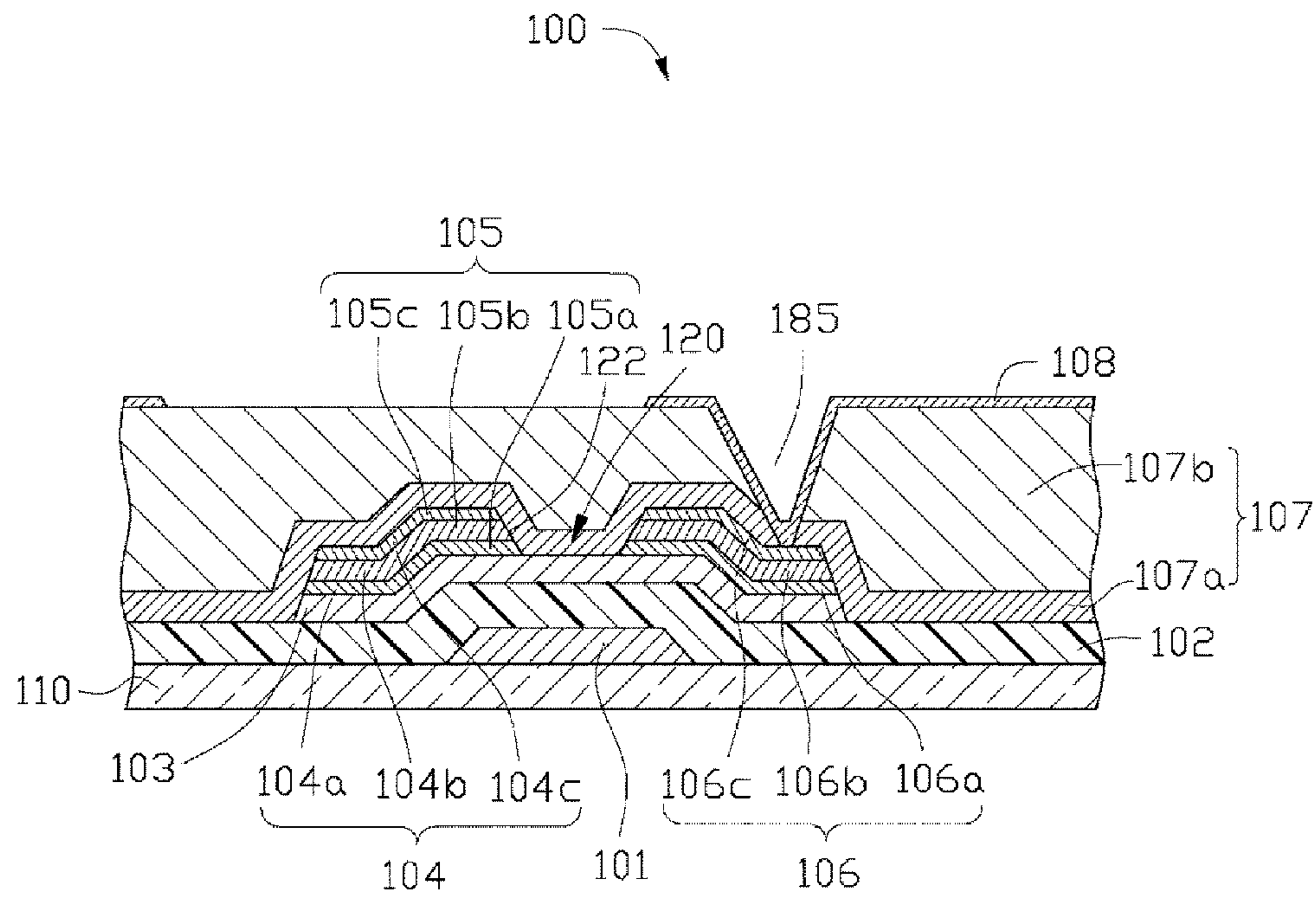
[Fig. 1]



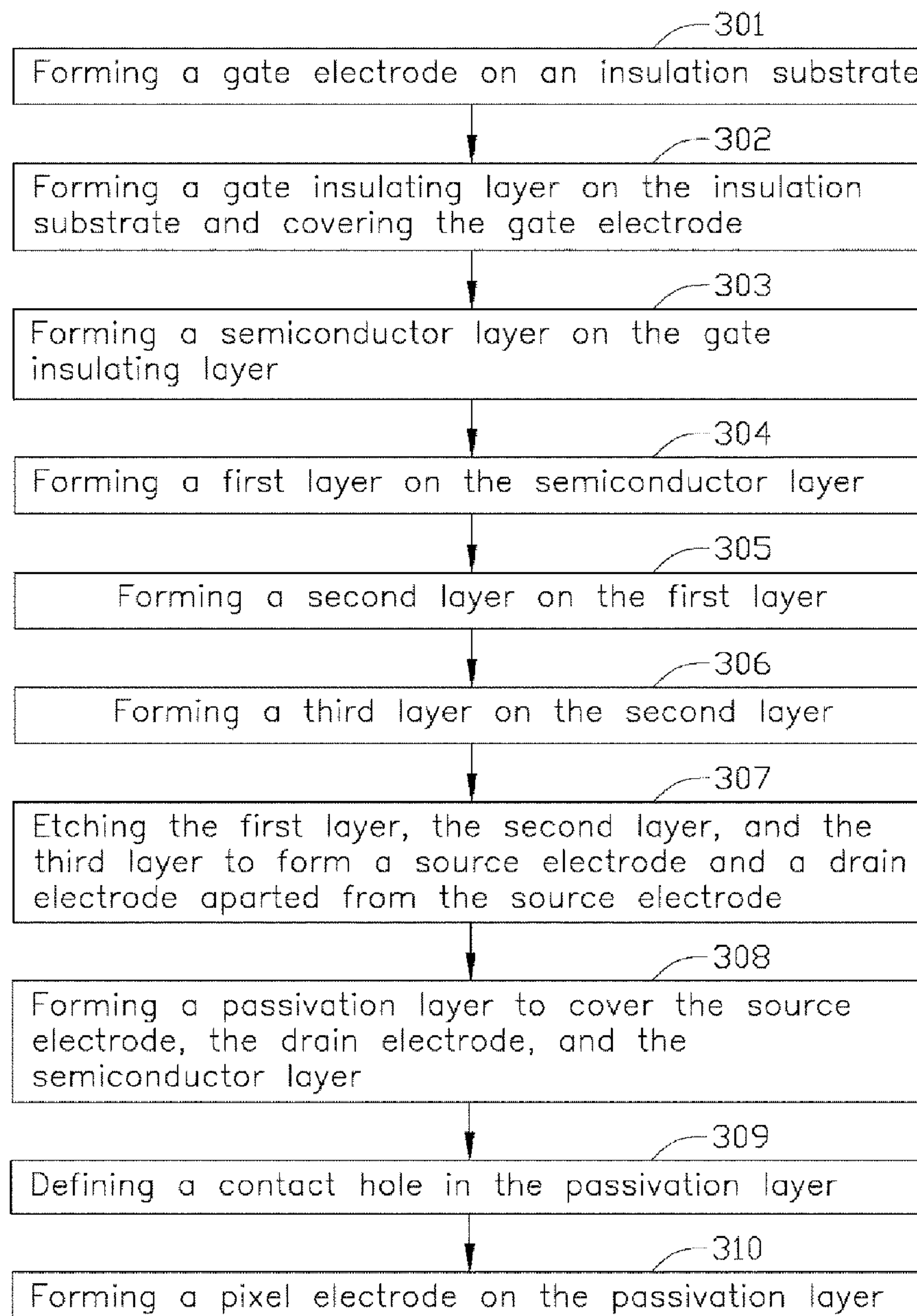
[Fig. 2]



[Fig. 3]



[Fig. 4]



TFT SUBSTRATE AND METHOD FOR MAKING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority from U.S. provisional application Ser. Nos. 62/268,474 filed on Dec. 16, 2015, and 62/278,469 filed on Jan. 14, 2016 which are incorporated herein by reference.

FIELD

The subject matter herein generally relates to a thin film transistor (TFT) array substrate, and method for making the TFT substrate.

BACKGROUND

In a flat panel display, a TFT, which is a three-terminal element, is used as the switching element. A gate line transfers a scanning signal for controlling the thin film transistor, a data line transfers a data signal applied to a pixel electrode, as well as other elements are included in the flat panel display. To provide better color accuracy and display response time, a high-performance TFT is needed in a panel display. Therefore, there is room for improvement in the art.

BRIEF DESCRIPTION OF THE DRAWINGS

Implementations of the present technology will now be described, by way of example only, with reference to the attached figures.

FIG. **1** is a circuit diagram of a portion of a TFT substrate.

FIG. **2** is a cross-sectional view of an exemplary embodiment of the TFT substrate of FIG. **1**.

FIG. **3** is a cross-sectional view of an exemplary embodiment of the TFT substrate of FIG. **1**.

FIG. **4** is a flow chart of a method for making the TFT substrate of FIG. **3**.

DETAILED DESCRIPTION

It will be appreciated that for simplicity and clarity of illustration, where appropriate, reference numerals have been repeated among the different figures to indicate corresponding or analogous elements. In addition, numerous specific details are set forth in order to provide a thorough understanding of the embodiments described herein. However, it will be understood by those of ordinary skill in the art that the embodiments described herein can be practiced without these specific details. In other instances, methods, procedures, and components have not been described in detail so as not to obscure the related relevant feature being described. Also, the description is not to be considered as limiting the scope of the embodiments described herein. The drawings are not necessarily to scale and the proportions of certain parts have been exaggerated to better illustrate details and features of the present disclosure.

Several definitions that apply throughout this disclosure will now be presented.

The term "coupled" is defined as connected, whether directly or indirectly through intervening components, and is not necessarily limited to physical connections. The connection can be such that the objects are permanently connected or releasably connected. The term "comprising," when utilized, means "including, but not necessarily limited to"; it specifically indicates open-ended inclusion or membership in the so-described combination, group, series, and the like.

FIG. **1** through FIG. **3** illustrate a TFT substrate **100**. As shown in FIG. **2** and FIG. **3**, the TFT substrate **100** includes an insulation substrate **110** and a first conductive layer **130** formed on the insulation substrate **110**. The first conductive layer **130** includes a plurality of scanning lines **121** and a plurality of gate electrodes **101** electrically coupled to the plurality of scanning lines **121**. FIG. **1** to FIG. **3** show, as an example, only one gate electrode **101** and two scanning lines **121**.

The insulation substrate **110** typically comprises an insulating material. Suitable materials for the insulation substrate **110** may include glass, quartz, plastic, and other materials having sufficient optical transparency (e.g., for visual display applications). In some embodiments, the insulation substrate **110** may comprise ceramic and/or silicon materials. In some applications, flexible substrate materials may be adopted. Suitable materials for the flexible substrate may include, for example, polyethersulfone (PES), polyethylene naphthalate (PEN), polyethylene (PE), polyimide (PI), polyvinyl chloride (PVC), and polyethylene terephthalate (PET) or combinations thereof.

Each scanning line **121** is configured to transmit gate signals. Each scanning line **121** extends mainly in a transverse direction, as shown in FIG. **1**. The scanning lines **121** and gate electrodes **101** are made of a same material. For example, the scanning lines **121** and gate electrodes **101** may be formed of one of aluminum (Al), copper (Cu), molybdenum (Mo), titanium (Ti), nickel (Ni), tungsten (W), gold (Au), palladium (Pd), platinum (Pt), chromium (Cr), neodymium (Nd), zinc (Zn), cobalt (Co), manganese (Mn), and any mixtures or alloys thereof. In addition, the scanning lines **121** and gate electrodes **101**, can comprise, for example, a transparent conductive material such as an indium tin oxide (ITO), an indium zinc oxide (IZO), and an aluminum doped zinc oxide (AZO).

As shown in FIG. **2** and FIG. **3**, the TFT substrate **100** further includes a gate insulating layer **102** on the first conductive layer **130**. The gate insulating layer **102** can be made of an electrically insulating material. For example, the gate insulating layer **102** may be made of silicon nitride (SiN_x), silicon oxide (SiO_x), silicon oxynitride (SiO_xN_y), aluminum oxide (AlO_x), yttrium oxide (Y_2O_3), hafnium oxide (HfO_x), zirconium oxide (ZrO_x), aluminum nitride (AlN), aluminum oxynitride (AlNO), titanium oxide (TiO_x), barium titanate ($BaTiO_3$), lead titanate ($PbTiO_3$), or a combination thereof.

For example, in at least one embodiment, the gate insulating layer **102** can be a single-layer structure, but is not limited thereto. The gate insulating layer may alternatively be formed as, for example, a double-layer structure.

As shown in FIG. **2** and FIG. **3**, the TFT substrate **100** further includes a semi-conductor layer **103** formed on the gate insulating layer **102**. The semiconductor layer **103** can comprise, for example, oxides of at least one of Zn, indium (In), tin (Sn), gallium (Ga), and hafnium (Hf). For example, in at least one embodiment, the semi-conductor layer **103** may be made of indium-gallium-zinc oxide (IGZO), indium-zinc-tin oxide (IZTO), indium-gallium-tin oxide (IGTO), or indium-aluminum-zinc oxide (IAZO).

As shown in FIG. **2**, the TFT substrate **100** further includes a second conductive layer **150** on the semiconductor layer **103** and the gate insulating layer **102**. The second conductive layer **150** includes a plurality of data lines **104**, a plurality of source electrodes **105**, and a plurality of drain

electrodes **106**. The plurality of source electrodes **105** and the plurality of drain electrodes **106** are separated from each other. FIG. **1** and FIG. **2**, as an example, show only one source electrode **105**, one drain electrode **106**, and two data lines **104**. Each data line **104** is configured to transmit data signals. Each data line **104** extends mainly in a longitudinal direction as shown in FIG. **1**, thereby intersecting the scanning lines **121**.

The second conductive layer **150** has a triple-layer structure and includes a first layer **151** positioned on the semiconductor layer **103**, a second layer **152** positioned on the first layer **151**, and a third layer **153** positioned on the second layer **152**. That is, each data line **104**, each source electrode **105**, and each drain electrode **106** have a triple-layer structure. Each data line **104** includes a first layer **104***a* positioned on the semiconductor layer **103**, a second layer **104***b* positioned on the first layer **104***a*, and a third layer **104***c* positioned on the second layer **104***b*. Each source electrode **105** includes a first layer **105***a* positioned on the semiconductor layer **103**, a second layer **105***b* positioned on the first layer **105***a*, and a third layer **105***c* positioned on the second layer **105***b*. Each drain electrode **106** includes a first layer **106***a* positioned on the semiconductor layer **103**, a second layer **106***b* positioned on the first layer **106***a*, and a third layer **106***c* positioned on the second layer **106***b*. The first layer **151** consists of the first layers **104***a*, **105***a*, and **106***a*. The second layer **152** consists of the second layers **104***b*, **105***b*, and **106***b*. The third layer **152** consists of the third layers **104***c*, **105***c*, and **106***c*.

The first layers **104***a*, **105***a*, and **106***a* are made of a same material and are made of metal oxide conductive material. The second layers **104***b*, **105***b*, and **106***b* are made of aluminum or an aluminum alloy. The third layers **104***c*, **105***c*, and **106***c* are made of a same material and are made of metal oxide conductive material. For example, the first layers **104***a*, **105***a*, and **106***a* may be made of one material selected from indium-zinc oxide, gallium-zinc oxide, and aluminum-zinc oxide. The third layers **104***c*, **105***c*, and **106***c* may be made of one material selected from indium-zinc oxide, gallium-zinc oxide, and aluminum-zinc oxide.

A groove **120** is formed between the source electrode **105** and the drain electrode **106** separating the source electrode **105** and the drain electrode **106** from each other. The groove **120** is formed by etching the second conductive layer **150**, the groove **120** passes through the first layer **151**, the second layer **152**, and the third layer **153**.

In this embodiment, the first layer **151** and the third layer **153** are made of metal oxides containing the same elements. That is, the first layer **151** and the third layer **153** are made of a same metal oxide. Both the first layer **151** and the third layer **153** contain zinc atoms. For example, both the first layer **151** and the third layer **153** are made of indium-zinc oxide. An atomic percentage of zinc in the third layer **153** is greater than an atomic percentage of zinc in the first layer **151**. As such, an etching rate of the third layer **153** is greater than an etching rate of the first layer **151**. In this embodiment, the third layer **153** has an etching rate which is greater than that of the second layer **152**, and the second layer **152** also has an etching rate which is greater than that of the first layer **151**. When the second conductive layer **150** is etched to form the groove **120**, the groove **120** includes a side wall **122** which is inclined towards the semiconductor layer **103**. The size of the groove **120** gradually decreases along a direction from the third layer **153** towards the first layer **151**. The etching rates of the first layer **151**, the second layer **152**, and the third layer **153** are determined under the condition of the second conductive layer **150** being etched by using a single etching solution or a single etching gas.

The first layer **105***a* can function as an ohmic contact layer between the semiconductor layer **103** and the second layer **105***b*; and the first layer **106***a* can function as an ohmic contact layer between the semiconductor layer **103** and the second layer **106***b*.

In other exemplary embodiments, the third layers **104***c*, **105***c*, and **106***c* can be omitted. That is, each data line **104**, each source electrode **105**, and each drain electrode **106** can have a double-layer structure. Each data line **104** includes a first layer **104***a* and a second layer **104***b* positioned on the first layer **104***a*. Each source electrode **105** includes a first layer **105***a* positioned on the semiconductor layer **103** and a second layer **105***b* positioned on the first layer **105***a*. Each drain electrode **106** includes a first layer **106***a* positioned on the semiconductor layer **103** and a second layer **106***b* positioned on the first layer **106***a*. The groove **120** passes through the second layer **152** and the first layer **151**, the size of the groove **120** gradually decreasing along a direction from the second layer **152** towards the first layer **151**.

One gate electrode **101**, one source electrode **105**, one drain electrode **106**, and one semiconductor layer **103** cooperatively form a TFT. A portion of the semiconductor layer **103** between the source electrode **105** and the drain electrode **106** defines a channel region of the TFT.

As shown in FIG. **3**, the TFT substrate **100** further includes a passivation layer **107**. The passivation layer **107** covers the source electrodes **105**, the drain electrodes **106**, the data lines **104**, and the semiconductor layers **103**. The passivation layer **107** may be made of, for example, an inorganic insulator such as silicon nitride or silicon oxide, an organic insulator, or a low dielectric ratio insulator. For example, the passivation layer **107** may be formed of an organic insulator such as polyimide, polyamide, acrylic resin, epoxy resin, cyclo-olefin resin, or BCB (benzocyclobutene).

In at least one embodiment, the passivation layer **107** may comprise, for example, a lower passivation layer **107***a* and an upper passivation layer **107***b*. For example, the lower passivation layer **107***a* may be made of silicon oxide and the upper passivation layer **107***b* may be made of silicon nitride.

The passivation layer **107** defines a plurality of contact holes **185** passing through the passivation layer **107**. FIG. **2** shows only one contact hole **185**. An end of the drain electrode **106** is exposed by the contact hole **185**.

As shown in FIG. **3**, the TFT substrate **100** further includes a plurality of pixel electrodes **108** formed on the passivation layer **107**. FIG. **2** shows one pixel electrode **108**. Each pixel electrode **108** is physically and electrically connected to a drain electrode **106** through a contact hole **185**, thereby receiving a data voltage from a drain electrode **106**.

The pixel electrode **108** may be made of a transparent conductor such as, for example, indium tin oxide (ITO), indium zinc oxide (IZO), aluminum zinc oxide (AZO), cadmium tin oxide (CTO), or a reflective electric conductor such as, for example, aluminum (Al), gold (Au), silver (Ag), copper (Cu), iron (Fe), titanium (Ti), tantalum (Ta), molybdenum (Mo), rubidium (Rb), tungsten (W), and alloys, or combinations thereof. Additionally, the pixel electrode **108** can be formed of, for example, transflective materials or a combination of transparent materials and reflective materials. In other embodiment, the pixel electrode **108** can be an organic light emitting diode (OLED) bottom electrode.

FIG. **4** illustrates a flow chart of an exemplary method for making the TFT substrate **100** shown in FIG. **3**. The method

is provided by way of example, as there are a variety of ways for carrying out the method. Each block shown in FIG. **4** represents one or more processes, methods, or subroutines, carried out in the exemplary method. The exemplary method can begin at block **301**.

At block **301**, an insulation substrate **110** is provided and a gate electrode **101** is formed on the insulation substrate **110**. At least one scanning line **121** is electrically coupled to the gate electrode **101** and may also be formed together with the gate electrode **101**. The method of forming of the gate electrode **101** and the scanning line **121** may include: depositing a first conductive material layer (not shown) on the insulation substrate **110**, and etching and patterning the first conductive material layer to form the gate electrode **101** and the scanning line **121**.

At block **302**, a gate insulating layer **102** is formed on the insulation substrate **110** and covers the gate electrode **101**.

At block **303**, a semiconductor layer **103** is formed on the gate insulating layer **102**.

At block **304**, a first layer **151** is formed on the semiconductor layer **103**. The first layer **151** can be made of metal oxide.

At block **305**, a second layer **152** is formed on the first layer. The second layer **152** can be made of aluminum or aluminum alloy.

At block **306**, a third layer **153** is formed on the second layer. The third layer **153** can be made of metal oxide.

At block **307**, the first layer **151**, the second layer **152**, and the third layer **153** are etched to form a source electrode **105**, a drain electrode **106**, and at least one data lines **104**. A groove **120** is formed during the etch process and the groove **120** passes through the first layer **151**, the second layer **152**, and the third layer **153**. The source electrode **105** is spaced apart from the drain electrode **106** by the groove **120**. The size of the groove **120** gradually decreases along a direction from the third layer **153** to the first layer **151**.

At block **308**, a passivation layer **107** is formed to cover the source electrode **105**, the drain electrode **106**, and the semiconductor layer **103**.

At block **309**, a contact hole **185** is defined in the passivation layer **107**. The contact hole **185** corresponds to the drain electrode **106** and passes through the passivation layer **107**.

At block **310**, a pixel electrode **108** is formed on the passivation layer **107**. The pixel electrode **108** also extends into the contact hole **185** to electrically couple to the drain electrode **106**.

The embodiments shown and described above are only examples. Many details are often found in the art such as other features of a display device. Therefore, many such details are neither shown nor described. Even though numerous characteristics and advantages of the present technology have been set forth in the foregoing description, together with details of the structure and function of the present disclosure, the disclosure is illustrative only, and changes may be made in the detail, especially in matters of shape, size, and arrangement of the parts within the principles of the present disclosure, up to and including the full extent established by the broad general meaning of the terms used in the claims. It will therefore be appreciated that the embodiments described above may be modified within the scope of the claims.

The invention claimed is:

1. A TFT substrate comprising:

a substrate;

a semiconductor layer formed on the substrate, the semiconductor layer having a top surface and a bottom surface opposite to and facing away from the top surface;

a first conductive layer formed on the bottom surface of the semiconductor layer, the first conductive layer defining a gate electrode; and

a second conductive layer formed on the top surface of the semiconductor layer opposite to the first conductive layer, the second conductive layer defining a source electrode and a drain electrode spaced apart from the source electrode;

wherein the second conductive layer comprises a first layer positioned on the semiconductor layer, a second layer positioned on the first layer, and a third layer positioned on the second layer; the second layer is made of aluminum; both the third layer and the first layer are made of a same metal oxide; an etching rate of the third layer is greater than an etching rate of the first layer when the second conductive layer is etched by a single etching solution or a single etching gas;

wherein both the third layer and the first layer are made of a same metal oxide containing zinc; the third layer has an atomic percentage of zinc greater than that of the first layer.

2. The TFT substrate of claim **1**, wherein a groove is defined between the source electrode and the drain electrode; the groove extends through the first layer, the second layer, and the third layer; and wherein the size of the groove gradually decreases along a direction from the third layer to the first layer.

3. The TFT substrate of claim **1**, further comprising a gate insulator layer, wherein the gate insulating layer is formed on the substrate and covers the gate electrode; and the semiconductor layer is formed on the gate insulating layer.

4. The TFT substrate of claim **1**, further comprising a passivation layer covering the semiconductor layer and the second conductive layer.

5. The TFT substrate of claim **4**, further comprising a pixel electrode on the passivation layer, wherein the pixel electrode is electrically coupled to the drain electrode.

6. A method for making a TFT substrate comprising:

forming a gate electrode on a substrate;

forming a gate insulating layer on the substrate and covering the gate electrode;

forming a semiconductor layer on the gate insulating layer;

forming a first layer on the semiconductor layer, the first layer being made of a metal oxide;

forming a second layer on the first layer, the second layer being made of aluminum;

forming a third layer on the second layer, the third layer being made of a same metal oxide with the first layer; and

etching the first layer, the second layer, and the third layer to form a source electrode and a drain electrode spaced apart from the source electrode; wherein an etching rate of the third layer is greater than an etching rate of the first layer;

wherein both the third layer and the first layer are made of a same metal oxide containing zinc; and the third layer has an atomic percentage of zinc greater than that of the first layer.

7. The method of claim **6**, wherein a groove is formed between the source electrode and the drain electrode; the groove extends through the first layer, the second layer, and

the third layer; and wherein the size of the groove gradually decreases along a direction from the third layer to the first layer.

8. The method of claim **6**, further comprising a step of forming a passivation layer covering the semiconductor layer and the third layer.

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