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[54] METHOD OF FORMING SEMICONDUCTING MATERIALS AND BARRIERS USING A MULTIPLE CHAMBER ARRANGEMENT

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[*] Notice: The portion of the term of this patent subsequent to Feb. 16, 2010, has been disclaimed.

[21] Appl. No.: **949,753**

[22] Filed: **Sep. 23, 1992**

Related U.S. Application Data

[60] Continuation of Ser. No. 639,197, Mar. 11, 1991, Pat. No. 5,187,115, which is a division of Ser. No. 394,281, Aug. 16, 1989, Pat. No. 5,049,523, which is a continuation of Ser. No. 180,720, Apr. 4, 1988, abandoned, which is a continuation of Ser. No. 935,606, Dec. 1, 1986, abandoned, which is a continuation of Ser. No. 716,409, Mar. 27, 1985, abandoned, which is a division of Ser. No. 355,202, Mar. 5, 1982, abandoned, which is a division of Ser. No. 88,100, Oct. 24, 1979, Pat. No. 4,328,258, which is a division of Ser. No. 857,690, Dec. 5, 1977, Pat. No. 4,226,897.

[51] Int. Cl.⁶ **H01L 21/00; H01L 21/02; H01L 21/20**

[52] U.S. Cl. **437/101; 427/569; 118/719**

[58] Field of Search **437/101, 113, 437/173; 118/719; 427/569**

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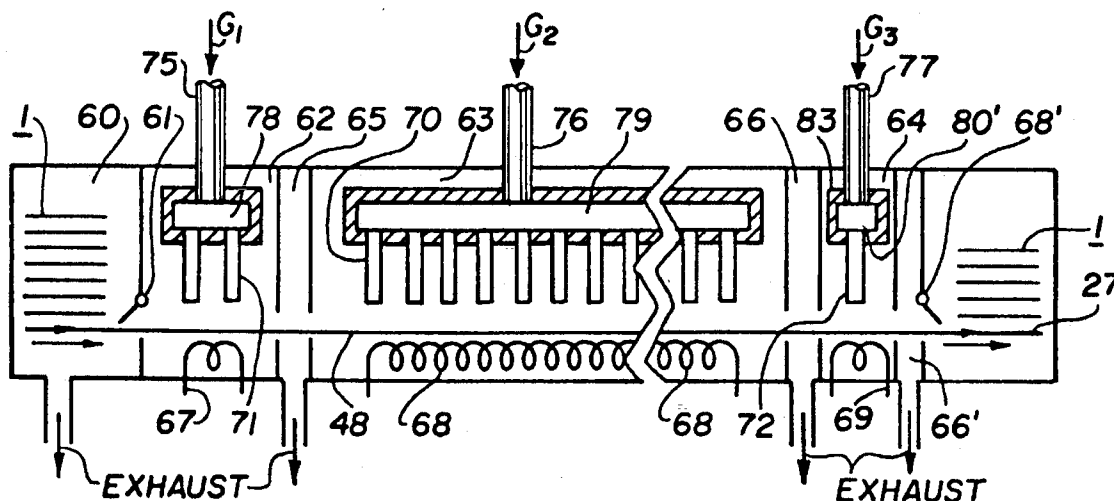
Primary Examiner—R. Bruce Breneman

Assistant Examiner—Byron Everhart

[57] ABSTRACT

In a gaseous glow-discharge process for coating a substrate with semiconductor material, a variable electric field in the region of the substrate and the pressure of the gaseous material are controlled to produce a uniform coating having useful semiconducting properties. Electrodes having concave and cylindrical configurations are used to produce a spatially varying electric field. Twin electrodes are used to enable the use of an AC power supply and collect a substantial part of the coating on the substrate. Solid semiconductor material is evaporated and sputtered into the glow discharge to control the discharge and improve the coating. Schottky barrier and solar cell structures are fabricated from the semiconductor coating. Activated nitrogen species is used to increase the barrier height of Schottky barriers.

34 Claims, 3 Drawing Sheets



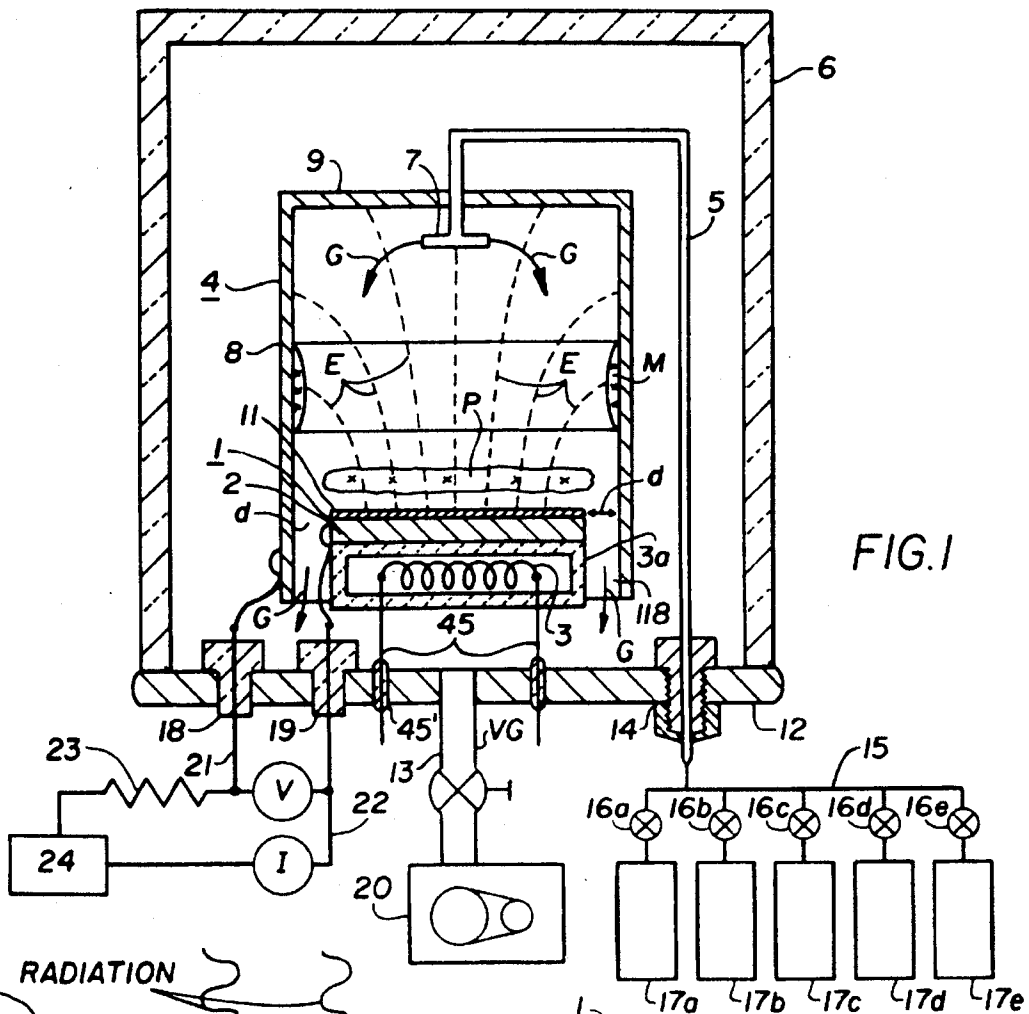


FIG. 1

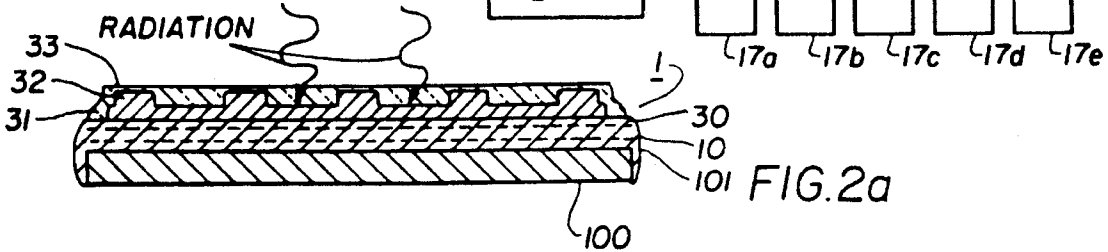


FIG. 2a

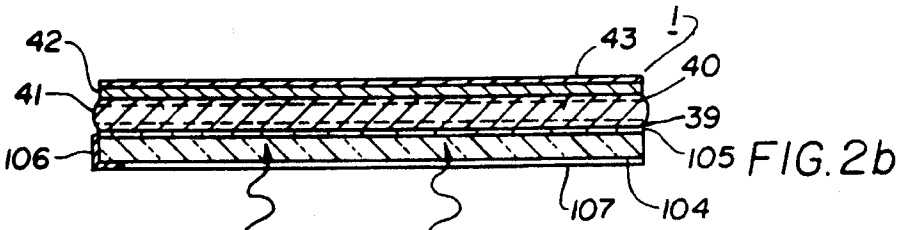


FIG. 2b

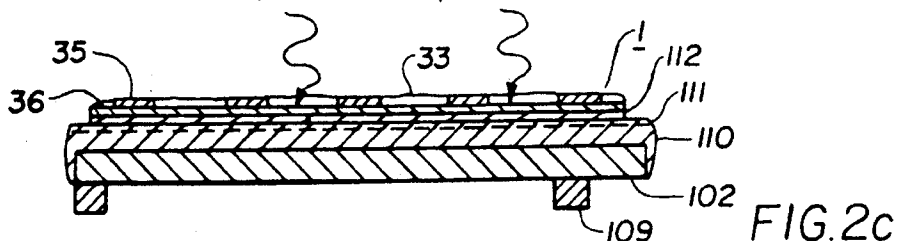
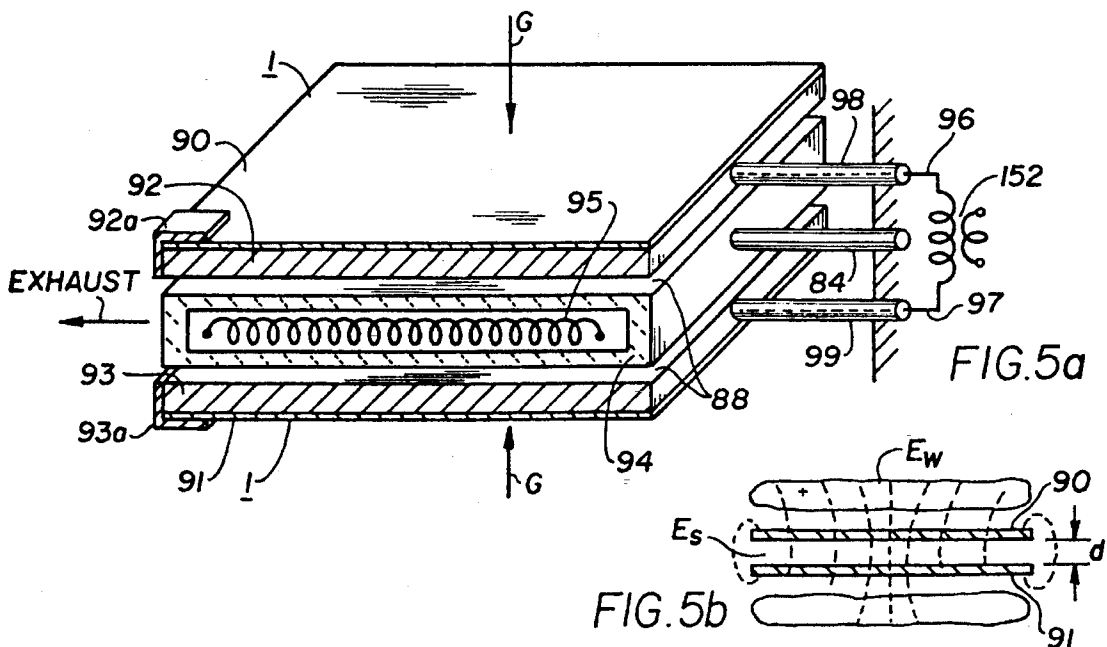
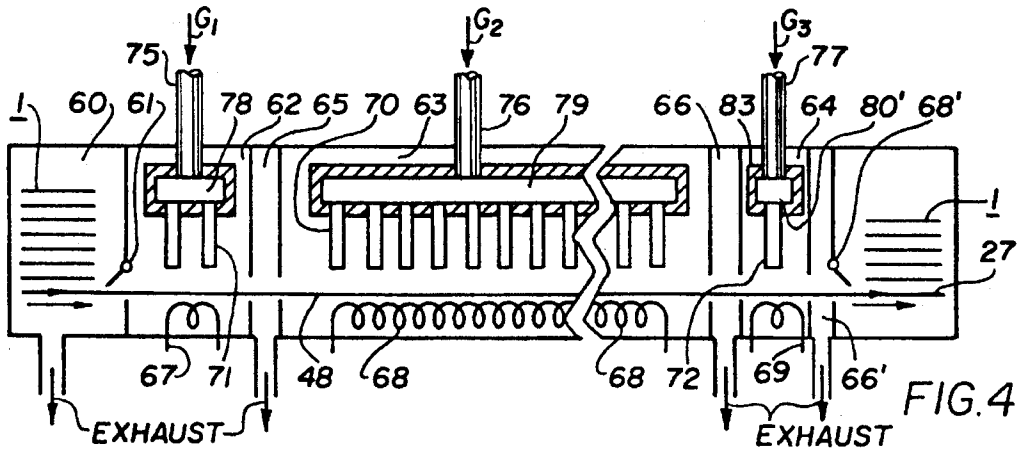
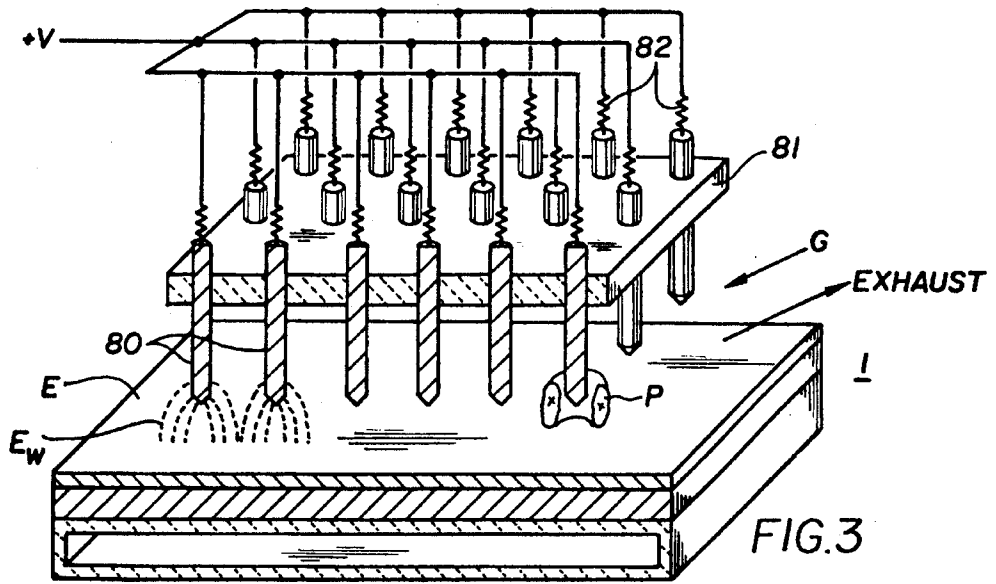
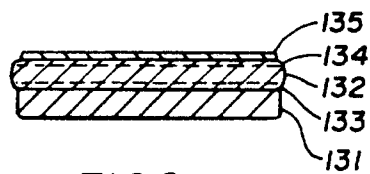
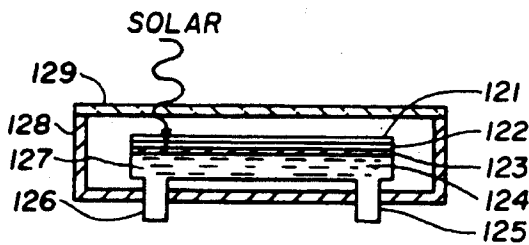
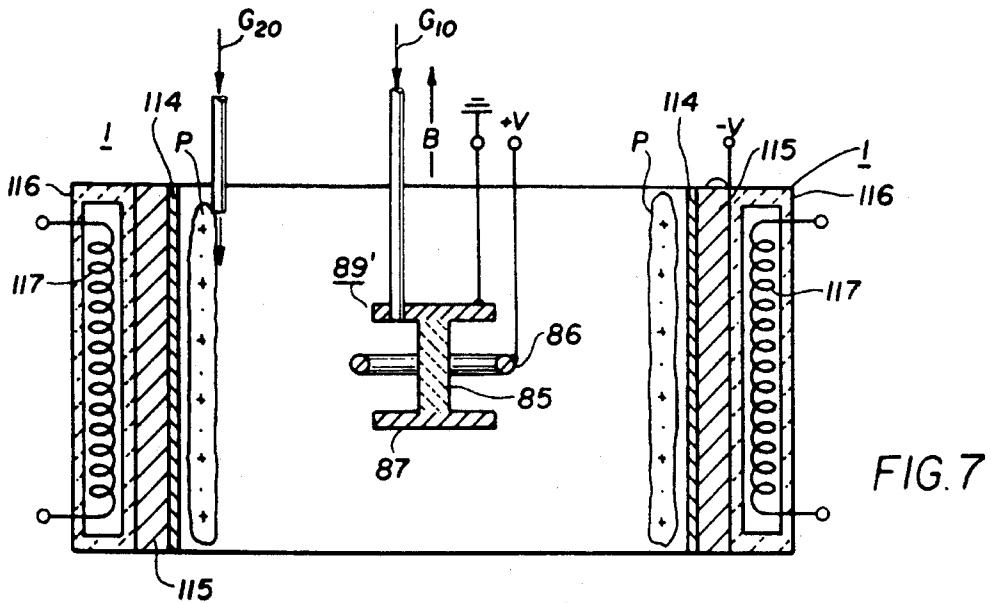
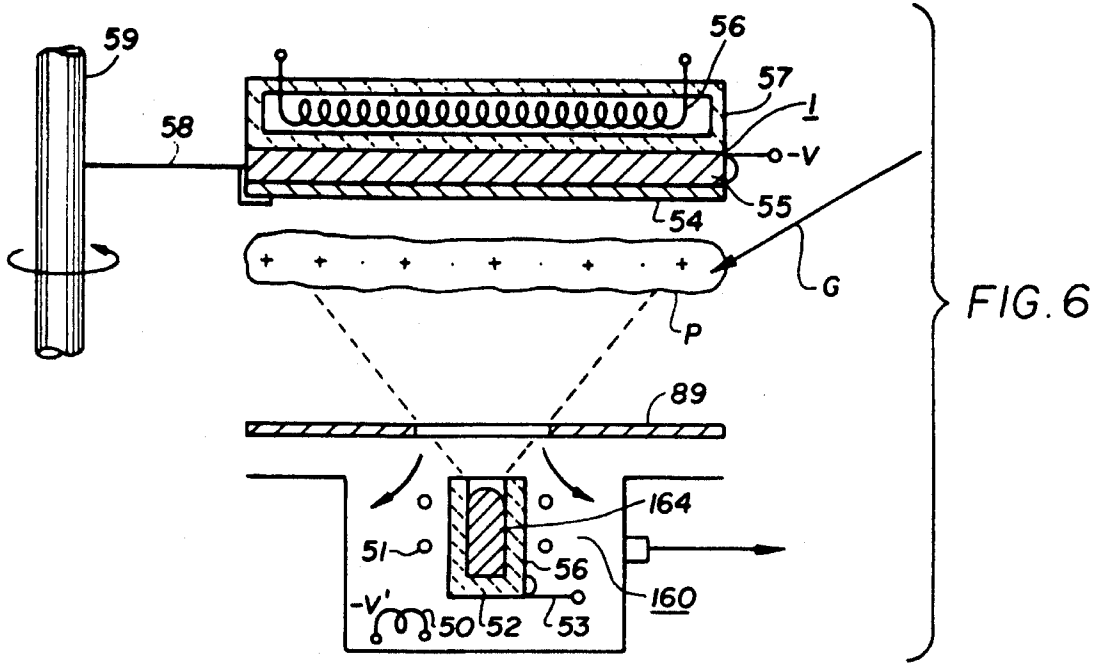


FIG. 2c





**METHOD OF FORMING
SEMICONDUCTING MATERIALS AND
BARRIERS USING A MULTIPLE CHAMBER
ARRANGEMENT**

This application is a continuation of Ser. No. 07/639,197 filed Mar. 11, 1991, which is a division of Ser. No. 07/394,281 Aug. 16, 1989 now (U.S. Pat. No. 5,049,523) which is a continuation of 07/180,720, Apr. 4, 1988 now abandoned, which is a continuation of 06/935,606, Dec. 1, 1986 now abandoned, which is a continuation of 06/716,409, Mar. 27, 1985 now abandoned, which is a division of 06/355,202 Mar. 5, 1982 now abandoned, which is a division of 06/088,100, Oct. 24, 1979 now (U.S. Pat. No. 4,328,258) which is a division of 05/857,690, Dec. 5, 1977 now (U.S. Pat. No. 4,226,890).

BACKGROUND OF THE INVENTION

Hydrogenated amorphous silicon films, hereinafter called a-Si, which are suitable for semiconductor applications have been prepared by a variety of techniques. Chittick, Alexander, and Sterling reported in the *Journal of the Electrochemical Society*, Vol 116, No. 1 (January 1969) pages 77-81, in an article entitled "The Preparation and Properties of Amorphous Silicon", that an inductively coupled, RF glow-discharge in silane (SiH₄) gas produced low-conductivity a-Si films that could be doped with both donor and acceptor impurities, thereby changing the a-Si conductivity over a wide range of values. More recently, a-Si films were produced by evaporating silicon in an atmosphere of hydrogen (H₂) and by sputtering silicon in an atmosphere of H₂+Ar which exhibited similar semiconductor characteristics to those films made from silane in a glow-discharge.

Presently, several commercial projects related to the development of Schottky barrier solar cells using crystal, polycrystal, and amorphous semiconductor materials were described in a recent book entitled *Twelfth IEEE Photovoltaic Specialists Conference-1976*, published by the Institute of Electronic and Electrical Engineers Inc., New York, N.Y., 10017. On pages 893-895 of this book, Carlson et al reported in an article entitled "Solar Cells Using Schottky Barriers on Amorphous Silicon" that he formed a solar cell by applying a transparent electrode with appropriate work-function to one side of an a-Si film and an ohmic contact to the other. Also, this article stated output voltages increased initially by 100 mV when the thin metal electrode was evaporated in residual oxygen background in the vacuum system, producing a metal-insulator-semiconductor (MIS) structure. More recently, Carlson reported in Vol 77-2 *Extended Abstracts, Fall Meeting, Atlanta, Georgia, Oct. 9-14 1977* of the Electrochemical Society, Princeton, N.J., 08540, pages 791-792, that these MIS cells were generally unstable. Furthermore, Carlson reported that his electrodes were less than 0.02 cm² in area—a value too small for commercial use. Also, an article by Godfrey & Green in *Applied Physics Letters* Vol 31, No. 10, (15 Nov. 1977) pages 705-707, indicates that such small areas lead to erroneous data.

My prior glow-discharge coating processes are covered in U.S. Pat. Nos. 3,068,283, 3,068,510 (Dec. 18, 1962) and 3,600,122 (Aug. 17, 1971). These processes generally related to polymeric coatings which have resistivities greater than 10¹² ohm-cm. High-resistivity coatings act as blocking capacitance in series with the glow-discharge thereby assisting in regulation of coating uniformity. However, neither 60 Hz line transformers nor DC power supplies can be used

with my prior processes. The present process, on the other hand, produce semiconducting films which act primarily as resistances in series with the glow discharge and which require different process concepts.

SUMMARY OF THE INVENTION

The present coating process is related to producing semiconductor films which have electrical resistivities generally greater than about 10¹² ohm-cm at room-temperature, and preferably between 10¹² and 10⁶ ohm-cm. The present process is designed to produce uniform semiconducting coating over a large area by means of a glow-discharge in which pressure and electric field are controlled. Also, the present process relates to the treatment of a semiconductor surface to increase the Schottky barrier voltage when an active conducting coating is applied. Such treatment may be used on any semiconductor material, including crystal semiconductors which have conductivities of 100 and 0.01 ohm cm. and higher. My coating process and barrier treatment is particularly useful for producing a Schottky barrier solar cell.

The principle object of the process is to produce a semiconductor and barrier for use in a solar cell. Another object of the invention is to coat a large-area substrate with amorphous semiconducting material. Yet another object is to form a Schottky barrier between a semiconducting material and an active electrode. Another object is to dope large area amorphous semiconductor materials to form an ohmic contact with a conducting substrate. Another object is to introduce semiconductor material from a solid-source into a coating being formed by glow-discharge deposition from the gas-phase.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a cross-sectional view of apparatus illustrating glow-discharge in the weak electric field.

FIG. 2 is a cross-sectional view of devices using semiconductor material produced in a glow-discharge and treated with activated nitrogen.

FIG. 3 illustrates another embodiment of the invention in which multiple electrodes are employed to maintain a glow-discharge.

FIG. 4 illustrates another embodiment in which the substrate is moved through the glow-discharge.

FIG. 5 illustrates another embodiment in which the electric field configuration and pressure are adjusted to enable alternating voltages to be applied while collecting a substantial part of the semiconducting material.

FIG. 6 illustrates another embodiment in which semiconductor material is evaporated through the glow-discharge to stabilize the discharge and attain desired semiconducting properties.

FIG. 7 illustrates another embodiment in which semiconductor material is sputtered through the glow-discharge to stabilize the discharge and attain desired semiconductor properties.

FIGS. 8-9 illustrates applications of films made in accordance with the present invention

**DESCRIPTION OF THE APPARATUS AND
TECHNIQUES**

Referring to FIGS. 1 and 2a, cross-sectional views are illustrated of the glow-discharge apparatus and a typical

device made therein. The substrate 1 is a 0.010" thick stainless-steel plate 11 with rectangular dimensions of 3"x4" supported by electrode 2. Resistance heater 3 is embedded in ceramic block 3a which supports and heats electrodes 2, 11. Substrate 1 is positioned in the open face of concave counter electrode 4 which has a rectangular cross-section of 4"x5" defined by side-walls 8 and top 9. Top 9 is positioned at least 4½" above the front surface of substrate 11. Electrode assemblies 1 and 4 are positioned inside an enclosure 6 and header 12 and are joined by appropriate gasket to form a gastight seal. Vacuum pump 20 is connected through valve and nipple 13 to header 12 to evacuate enclosure 6. Gases G from tanks 17 a-e are conducted through regulated needle valves 16 a-e, manifold line 15, and connector 14 through header 12 into enclosure 6. Here, gases G are conducted through dielectric tubing 5 and diffuser 7 inside electrode 4. A gap 118 of say ½" between walls 8 and electrode 2 permits egress of gases G after passing through glow-discharge P. Guage VG meters the evaluation of enclosure 6 and pressure of gases G. Guage VG is preferably of the capacitance-manometer type which is commercially available for use with corrosive, condensable gases in the range of 0.001 to 10 Torr. Readings from guage VG may automatically regulate valves 16 through a servo-mechanism to maintain a desired pressure. A potential V is applied between electrodes 2, 4 from power supply 24 by leads 21, 22 connected through insulated electrical bushings 18, 19 sealed in header 12. Protective network 23 prevents damaging sparks. Voltage V and current I are metered as indicated. Resistance heater 3 enclosed in ceramic 3a is connected through leads 45 and electrical bushings 45' to an appropriate power source (not shown).

In operation, the enclosure 6 is evacuated by pump 20 to a pressure below about 0.02 Torr and back-filled with silane (SiH₄) from tank 17a by opening valve 16a. Valve 16a is adjusted to maintain the desired pressure in enclosure 6 which, for example, may be ½ Torr. Next a mixture of 10% phosphine (PH₃) in helium (He) from tank 17b is admitted into manifold 15 where it mixes with silane and flows through lines 5, 7 to raise the system pressure PG to about 1 Torr. The potential difference V between electrodes 2, 4 is adjusted to about 530 volts initiating a glow-discharge and the current, I adjusted to about 5 mA, to produce a heavily doped n⁺ coating 101 on plate 100. After maintaining the discharge for about 1 minute, valve 16b is closed to shut off the flow of PH₃ and He leaving silane alone. The uniformity and impurity level of ohmic-layer 101 is not as critical as that of the high-resistivity a-Si layer 10. Therefore, ohmic-layer 101 may be deposited by conventional, doped chemical-vapor-deposition (CVD) or other techniques, prior to insertion in the apparatus of FIG. 1.

Next, the pressure PG of silane is adjusted to 0.3 to 0.4 Torr to position a diffuse discharge P in the region above plate 100 and minimize the discharge in the region of closest separation d between electrodes 2, 4. The discharge then occurs in the weaker region of the electric-field E as will be discussed in more detail in connection with FIG. 5b. The discharge is maintained for 40 minutes at 5 mA with V in the range of 500-700 depending on PG. After desired thickness on substrate 1 is attained, valve 16b is closed and the residual gases evacuated to background by pump 20. Valve 16c on ammonia (NH₃) tank 17c is opened to admit NH₃ into the substrate region 1 to a pressure of about 400 Torr. A potential difference V is applied between electrodes 2, 4 of about 350 volts and I of 5 mA produce to a glow-discharge adjacent coated substrate 1. Valve 16c is closed, the residual gases in enclosure 6 evacuated by pump 20, and

the enclosure 6 is backfilled with nitrogen from tank 17d (valve 16d) to purge unreacted silane. Valve 13 is closed, jar 6 raised to atmospheric pressure and substrate 1 removed.

Referring to FIG. 2a, the substrate 1 is illustrated with foil 100 coated with n⁺-doped a-Si layer 101, undoped 1-4 μm a-Si layer 10 and ammonia-treated layer 30. The substrate 1 is then placed in a conventional vacuum-evaporator and coated with a high work-function, semi-transparent metal 31 (such as palladium) to a thickness of about 100 Å or less to complete the Schottky barrier. The conducting layer 31 is adjusted to be thick enough to reduce its sheet resistance while not absorbing an inordinate amount of incident photons. A grid 32 of thicker metal such as a silver-titanium alloy (Ag-Ti) is applied to reduce the series resistance of the semi-transparent electrode 31. Also, a top anti-reflection (AR) layer 33 such as Si₃N₄ with a thickness range of about 1000 Å may be applied to electrode 31 to reduce reflection loss under photon irradiation. Under test using AM1 illumination and a Tektronics Corp. curve tracer, the short-circuit current I_{sc} was measured to be about 2 mA/cm² and the open-circuit voltage Voc was about 350 mV, with no AR coating and 50% reflection loss. When the layer 30 was added by the NH₃ discharge, I_{sc} remained about 2 mA/cm² while the Voc was measured to be greater than 600 mv—an increase in excess of 250 mV, again with no AR coating. Similar increases were found with other substrates as illustrated in the following drawings.

Referring to FIG. 2b, a glass substrate 104 coated with a transparent conducting coating 105 of the oxides of indium (In) and tin (Sn) (commercially available) may be inserted into the apparatus of FIG. 1 on electrode 2 with the conducting coating 105 facing the discharge and conducting tab 106 contacting electrode 2. Thereafter, the coating procedure is the same as that described in connection with FIG. 2a, in that ohmic contact layer 39, a-Si layer 41, NH₃-treated barrier-layer 40 are produced sequentially. Also, using an evaporator, a Pd coating 42 is applied to complete the Schottky barrier and a thicker metallic layer 43 such as Ti-Ag applied to complete the contact. When substrate 1 is illuminated (in operation) through the glass substrate 104, electrode 43 may be opaque. An additional AR coating 107, such as an oxide of tantalum, may be applied to the glass. Although the glass substrate 104 serves as a useful protective material, the configuration of FIG. 2b produces somewhat less output than that of FIG. 2a since the maximum number of charge carriers are generated at the ohmic surface where the incident photons impinge first rather than at the barrier where the output potential is developed.

Referring again to FIG. 2a, b, p-type a-Si may be substituted for the n-type a-Si in coatings 10, 41 by doping with a donor impurity during formation in the apparatus in FIG. 1. For example, during formation of the a-Si coating 10, the apparatus of FIG. 1 may be operated as described above except that diborane from tank 17e (valve 16e) is added to the silane flow from tank 17b to dope the a-Si layer 10 to neutral or to p-type depending on the fractional amount of B/Si. Correspondingly, 1-10% diborane from tank 17e may be added to G to dope the ohmic-layer 101 to p⁺ level. For p-type a-Si, the active metal layer 31 is formed from a low work-function metal such as chromium (Cr) or aluminum (Al). In either case the layers 30, 40, may be formed by NH₃-discharge to enhance the Schottky barrier with any of the structures such as shown in FIG. 2a, b, c.

Referring again to the apparatus of FIG. 1, I found that barrier-height and Voc of an untreated a-Si material may be increased by glow-discharging in N₂ gas instead of NH₃. However, using the structure of FIG. 2a, when layer 30 was

formed from a N_2 discharge the increase in Voc amounts to only about 100 mV instead of 250 mV with NH_3 . Also, nitrogen atoms (N^*) produced an increased barrier. For example, using a commercial plasma torch producing a nitrogen atom beam to treat the surface **10**, Voc increased by 150 mV after 15 minutes treatment. This value is somewhat larger than the direct N_2 discharge but smaller than the 250 mV under direct NH_3 glow-discharge. Hydrazine proved more effective than N_2 alone. Air in an atomic beam was found to increase the Voc also; however, oxygen alone in a glow-discharge formed a blocking layer. The discharge for producing the NH_3 treated layer **30** is not as critical as that for producing the a-Si layer **10** since the gases, per se, do not form a film but combine with the coating **10**, deposited previously. The glow-discharge time-limits are determined by the limiting thickness through which charge carriers can tunnel.

Referring to FIG. 2c, the substrate **1** is 0.0035" thick stainless-steel foil **102** reinforced with frame **109** which may be 1/16" or thicker, to prevent foil **102** from bending in a small radius and damaging the a-Si film **110**. Again, a barrier layer **111** is formed by discharge treatment in ammonia. However, an additional barrier layer **112** is added which may be antimony trioxide (Sb_2O_3) or titanium dioxide (TiO_2) or other metallic oxides or nitrides having a thickness 50 Å or less to enhance the barrier height without blocking the desired charge carriers. In the case of TiO_2 , the semi-transparent layer **36** may be nickel (Ni) with a thickness 100 Å or less and may have an additional conducting layer of 50 Å or so of chromium (not shown). Contact fingers **35** and AR coating **33** are added to complete the photo-voltaic Schottky barrier. The cells of FIG. 2a, b, c may be made with any semiconductor material having a photoresponsive barrier such as that made in the following apparatus.

Referring to FIG. 3, the anode **4** of FIG. 1 is replaced by a set of cylindrical pins **80** supported by a dielectric holder **81**. Each pin **80** is connected through protective resistors **82** to +V. The surfaces of dielectric holder **81** and resistors **42** are positioned at least about 6" above the substrate **1** to avoid deposition of conducting silicon material (M noted in FIG. 1). Typical operating conditions are similar to those described in connection with FIG. 1 in that the desired gases G are admitted through a suitable distributor (not shown) and exhausted by a pump (not shown) except that the pressure and current density can be operated at higher values say up to 2 Torr and 1 mA/cm² and higher. Also, substrate **1** can be moved through the discharge for continuous coating or may remain static. Again, the fringing field lines E permit the discharge to move up the pins **80** by adjustment of pressure while maintaining the discharge in the weaker field E_w .

Other geometries can be used for pins **40** such as tapered pins or hollow cylinders facing the substrate **1**. Silicon which is collected on the pins **40** represents wasted material. However, I found that by applying DC or DC plus AC with the pins **40** biased anodically, silicon collection is minimized. For designing protective resistors **42**, if the average current densities (I/area) to substrate **1** is adjusted to be 0.2 mA/cm² and with pins **40** 1 cm apart, resistors may be in the range of 100 k ohms for good regulation. Hollow pins are described with a moving substrate in FIG. 4.

Referring to FIG. 4, an in-line system is illustrated schematically using hollow electrodes **70** with configuration similar to that in FIG. 3. A loading chamber **60**, airlock **61**, ohmic-layer deposition system **62**, and a-Si deposition-system **63** produce continuously coated substrates **1** such as those shown in FIG. 2a, b, c. Finally, chamber **64** treats the

coated substrate with activated ammonia species to form the barrier-layer. Appropriate gases **G1**, **G2**, **G3** are distributed through lines **75**, **76**, **77** into ceramic chambers **78**, **79**, and **80** which may conveniently house electrodes **71**, **72**, **73** respectively. The gases from distributors **78**, **79**, **80** flow through hollow pins **71**, **72**, **70** into pumping ports **65**, **66** and are exhausted by pumps (not shown). Pressures in ports **65**, **66** are adjusted to be below that in compartments **62**, **63**, **64** to insure that the exhaust gases G do not flow into adjacent compartments. In operation, the size of each compartment **62**, **63**, and **64** is adjusted for the discharge residence time to produce the desired coating thickness. Resistance heaters **67**, **68**, **69** maintain the substrate **1** at the desired temperature. The temperature of the substrate **1** in the a-Si region **63** should be between 200° and 350° C., whereas the temperature in the ohmic-layer region **62** can be considerably higher. The temperature in the NH_3 region **66** should be below about 300° to avoid dehydrogenation of the a-Si.

In operation, airlock **61** is closed and the substrate **1** which, for example, are one meter square stainless steel plates, are loaded in chamber **60** and the air is evacuated. Air lock **61** is opened and a commercial feeder mechanism (not shown) moves the substrate **1** along guide-rail **48** which acts as the electrical connection to ground for substrate **1**. Suitable mechanical mechanisms include individual moving armatures, endless conveyor belts and ultrasonic walkers. Substrate **1** is unloaded and collected in a stacking mechanism (not shown) in compartment **27**. Air lock **68** is closed and coated substrates **1** moved to the evaporation system as described in connection with FIG. 1. Alternatively, loading and unloading compartments **60**, **27** could be replaced with continuous seals, which are standard in the vacuum coating industry, to provide vacuum to air operation. Other suitable electrode configurations such as those described in FIG. 5 may be used with a moving substrate.

Referring to FIG. 5a, the preferred embodiment, electrodes are illustrated which enable the use of AC and efficient collection on the substrate **1** of a substantial part of the a-Si. Parallel, rectangular electrodes **92**, **93** hold stainless steel plates **90**, **91** forming substrate assembly **1**. End tabs **92a**, **93a** on electrodes **92**, **93** insure good electrical contact to substrates **90**, **91** and may act as guides if substrates **90**, **91** are moved during deposition. Electrical contact to electrodes **92**, **93** is made by leads **96**, **97** having ceramic insulators **98**, **99**. Leads **96**, **97** are connected to center-tapped transformer **152**. The plates may be supported by leads **96**, **97** and additional insulators (not shown). Electrodes **92** are heated, for simplification of the illustration, by resistance-heater **95**, ceramic insulation **94**, and supported by a suitable ceramic rod **84**. A small gap **88** is maintained between heater insulation **94** and electrodes **92**, **93** to avoid short-circuiting electrodes **92**, **93** through conducting Si, which deposits on insulation **94**. Also, dielectric members **98**, **99**, and **84** should extend a distance greater than about 6" from the region of electrodes **90**, **91** under glow-discharge. Input gases G are distributed and exhausted from lines (not shown) as described in connection with FIG. 1.

In operation, silane gas G is admitted to a pressure of about 0.4 Torr and, when electrodes **92**, **94** have a minimum separation of 1/2", RMS voltage of about 650 volts between electrodes **90**, **91** from 60 Hz transformer **152** produces a current of 5 mA or about 0.2 mA/cm². These operating values are similar to those used with the DC supply of FIG. 1, except that each plate **90**, **91** becomes cathodic alternately. As illustrated in FIG. 5b, the negative glow encircles plates **90**, **91** in the weak electric field E_w and; for 1/2" separation

d, a silane pressure of 0.35 Torr eliminates all glow-discharge in the strong field E_s . The actual operating pressure of 0.40 Torr allows some discharge to the inactive ends. The pressure used during deposition of the ohmic-layer and NH_3 treatment is determined separately.

In practice, I found that transformer 152 of the neon-sign type was convenient for developmental-size models. In production, larger, self-regulating SCR, or saturable reactor transformers can be used. Line frequencies (50–60 Hz) and audio frequencies to 20K Hz, which are supplied from inexpensive solid state supplies, are the preferred power sources.

Referring to FIG. 6, an e-beam evaporation source 160 (commercially available) having an electron gun 50, magnetic deflector 51, and crucible 52 with electrical contact 53, is used to evaporate polycrystal (pxSi) 164 through a glow-discharge P onto substrate 1. Substrate 1 is comprised of stainless steel plate 54 retained on electrode 55 and heater 56 in ceramic enclosure 57 as discussed in connection with FIG. 1, however, electrodes 54, 55 are attached to arm 58 mounted on shaft 59. Shaft 59 may be rotated by a conventional mechanism (not shown) to move plate 54 from the coating region above source 160 to the vacuum metallization region (not shown) to apply electrodes as described in connection with FIG. 2a, b or the TiO_2 barrier layer, as described in connection with FIG. 2c. Baffle plate 89 and a high-capacity blower-pump (not shown) permit a low pressure in the evaporator region 160 and a higher pressure in the glow-discharge region P around substrate 1.

In operation, the crucible 56 may be grounded by lead 53 and a potential $-V$ is applied to substrate 1 to maintain the glow-discharge P in gases G. A negative potential $-V'$ may be applied to the e-beam source 50 to bombard and heat crucible 56, or other suitable heat sources may be used to heat crucible 56 to evaporate silicon 164. Evaporated Si passes through the glow-discharge P where it is partially ionized and joins the silane ions to coat the surface of plate 55. The evaporated material stabilizes the glow-discharge P and improves the semiconducting properties of the coating on plate 55. Gases G may be doped, undoped, or NH_3 as discussed in connection with FIG. 1. However, additional doping may be applied from the material in crucible 56. Also, any of the structures illustrated in FIGS. 2a, b, c may be formed and ammonia may be added without operating evaporation source 160.

Referring to FIG. 7, a sputtering source 89 of the inverted magnetron type such as I described with E. G. Linder and E. G. Apgar in *Proceedings of the IRE* (now IEEE) (July 1952), pages 818–828. The source 89 has a cylindrical electrode 85 composed of poly-crystal Si, end plates 87, anode ring 86, and magnetic field B with its principle component longitudinal to the axis of the electrode 85. The substrate 1 has plates 114, electrodes 115, heater dielectric 116 and element 117 similar to substrate 1 described in connection with FIG. 1. Substrate 1 is positioned to receive silicon sputtered from electrode 85. A potential $-V$ relative to ring 86 maintains a glow-discharge in input-gases G in the vicinity of the surface of plate 114.

In operation, gases G10 such as Ar or $Ar+H_2$ are injected between magnetron electrodes 85, 86. A suitable potential, $+V$, on anode 86 and magnetic field B are maintained to sputter silicon onto the surface of plate 114. At the same time, a potential $-V$ is applied to substrate 1 relating to electrode 85 to maintain a glow-discharge P in gases G10 and sputtered silicon from source 85. The potential $-V$ is maintained until the ions in glow-discharge P deposit on

substrate 114 to form a film of the desired thickness. Silicon from the sputter source 89 facilitates maintenance of a uniform glow-discharge in the vicinity of substrate 1 and improves conductivity characteristics of Schottky barriers such as illustrated in FIG. 2a, b, c.

Although I have used for convenience silane gases in the illustrations, other silicon-hydrogen gases can be used such as $SiHCl_3$ and SiH_2Cl_2 . Also, other semiconductor gases such as germane can be used to form hydrogenated amorphous germanium. Non-hydrogenated semiconductors can also be used with the present invention including the binary alloys of gallium. For example, trimethylgallium gas glow-discharged with several other gases forms semiconductor films with arsene, forms GaAs; with NH_3 , forms GaN; and, with PH_3 form GaP. Apparatus illustrating other devices utilizing such semiconductor films are shown in FIG. 5. and the other drawings.

Referring to FIG. 8, a solar thermal-collector is shown with a $1 \mu m$ a-Si film 121 and a-Ge film 123 coated on the front of stainless-steel plate 123 assembly which faces the solar radiation. Water 124, is circulated by input tubing 125 and output tubing 126 through enclosure 127 where it contacts the rear of plate 123. Transparent glazing 127, such as plate-glass, and enclosure 128 holds and insulates plate assembly 124 which is elevated in temperature by the solar radiation.

Under illumination, the visible solar radiation component which passes through glazing 12 is absorbed in the a-Si coating 121. The infra-red (IR) component of the solar radiation passes through the a-Si coating 121 and is absorbed in the a-Ge coating 122. Plate 123 preferably, has a polished or metallized surface with low IR emissivity for radiation wavelengths above say $2 \mu m$ —which would otherwise be radiated from the solar-heated plate 123, itself. Thus, the a-Si absorbs visible radiation whereas a-Ge, which has a smaller band gap than a-Si, absorbs the IR component. The a-Si, a-Ge films 121, 122 in combination yield close to the ideal characteristics of a solar thermal-collector-high absorptivity and low IR emissivity. Any of the processes described above may be used to coat the a-Si and a-Ge layers 121, 122. Also, the coated plate assembly 123 may be used separately without glazing 129 and box 128 as a selective surface in a focused collector (not shown). It should be noted that both a-Si and a-Ge formed in my apparatus absorb more efficiently than crystal Si or Ge, and cost substantially less than crystals. Another application of films made with the process is shown in FIG. 9.

Referring to FIG. 9, a p-n junction is shown with a stainless steel substrate 131 coated with a-Si film 132 which has a heavily doped n^+ layer making ohmic-contact with plate 131 as described in connection with FIG. 1. A p(or pp+) layer 134 is added to coating 132 forming a p-n junction. Top Cr contact layer 135 may be semi-transparent, if the device of FIG. 9 is operated as a solar cell. Alternate substrate 131 surfaces include alloys of antimony (Sb) and gold (Au).

Other applications of the coating process and the improved barrier-layer are field-effect-transistors FET, insulated-gate-field-effect-transistors IGFET, and charge-coupled-devices CCD.

I claim:

1. A process for glow discharge deposition in an apparatus comprising, a first deposition chamber adapted to be evacuated, first gas introducing means for introducing a first gaseous material into said first deposition chamber, first electrode means disposed in said first deposition chamber, a

second deposition chamber adapted to be evacuated, second gas introducing means for introducing a second gaseous material into said second deposition chamber, second electrode means disposed in said second deposition chamber, restricting means for restricting the flow of at least one of said gaseous materials from one of said deposition chambers into the other one of said deposition chamber, said restricting means being disposed between said first deposition chamber and said second deposition chamber, and transporting means for transporting said substrate from one of said deposition chambers to the other one of said deposition chambers through said restricting means, said process comprising the steps of:

disposing said substrate in said first deposition chamber; introducing said first gaseous material in said first deposition chamber and applying a first electric field to a first region in said first deposition chamber by said first electrode so as to generate a first glow discharge, whereby a first layer is deposited on said substrate;

transporting said substrate on which said first layer is deposited from said first deposition chamber to said second deposition chamber through said restricting means, while each interior of said deposition chambers is shielded from an external atmosphere; disposing said substrate on which said first layer is deposited in said second deposition chamber; and

introducing said second gaseous material in said second deposition chamber and applying a second electric field to a second region in said second deposition chamber by said second electrode so as to generate a second glow discharge, whereby a second layer is deposited on said first layer.

2. A process according to claim 1 wherein said first gaseous material comprises dopant gas and wherein said second gaseous material comprises a silane gas.

3. A process according to claim 2 wherein said dopant gas comprises phosphorus.

4. A process according to claim 1 wherein said first layer is a semiconductor layer comprising silicon and dopant and wherein said second layer is an intrinsic semiconductor layer comprising silicon.

5. A process according to claim 4 wherein said semiconductor layer comprises phosphorus and wherein said intrinsic semiconductor layer comprises hydrogenated amorphous silicon.

6. A process according to claim 1 wherein said first gaseous material comprises silicon and wherein said second gaseous material comprises nitrogen.

7. A process according to claim 1 wherein said first layer is a semiconductor layer comprising silicon and wherein said second layer comprises nitrogen.

8. A process according to claim 7 wherein said semiconductor layer comprises hydrogenated amorphous silicon.

9. A process for glow discharge deposition in an apparatus comprising, a first deposition chamber adapted to be evacuated, first gas introducing means for introducing a first gaseous material into said first deposition chamber, first electrode means disposed in said first deposition chamber, a second deposition chamber adapted to be evacuated, second gas introducing means for introducing a second gaseous material into said second deposition chamber, second electrode means disposed in said second deposition chamber, first restricting means for restricting the flow of at least one of said first and second gaseous materials from one of said first and second deposition chambers into the other one of said first and second deposition chambers, said first restricting means being disposed between said first deposition

chamber and said second deposition chamber, a third deposition chamber adapted to be evacuated, third gas introducing means for introducing a third gaseous material into said third deposition chamber, third electrode means disposed in said third deposition chamber, second restricting means for restricting the flow of at least one of said second and third gaseous materials from one of said second and third deposition chambers into the other one of said second and third deposition chambers said second restricting means being disposed between said second deposition chamber and said third deposition chamber, and transporting means for transporting a substrate, said process comprising the steps of:

disposing said substrate in said first deposition chamber; introducing said first gaseous material in said first deposition chamber and applying a first electric field to a first region in said first deposition chamber by said first electrode means so as to generate a first glow discharge, whereby a first layer is deposited on said substrate;

transporting said substrate on which said first layer is deposited from said first deposition chamber to said second deposition chamber through said first restricting means, while each interior of said deposition chambers is shielded from an external atmosphere;

disposing said substrate on which said first layer is deposited in said second deposition chamber;

introducing said second gaseous material in said second deposition chamber and applying a second electric field to a second region in said second deposition chamber by said second electrode so as to generate a second glow discharge, whereby a second layer is deposited on said first layer;

transporting said substrate on which said first layer and said second layer are deposited from said second deposition chamber to said third deposition chamber through said second restricting means, while each interior of said second and third deposition chambers is shielded from the external atmosphere;

disposing said substrate on which said first layer and said second layer are deposited in said third deposition chamber; and

introducing said third gaseous material in said third deposition chamber and applying a third electric field to a third region in said third deposition chamber by said third electrode means so as to generate a third glow discharge, whereby a third layer is deposited on said second layer.

10. A method of making a semiconductor device on a substrate comprising the steps of:

providing a first and second vacuum chambers;

evacuating said first and second vacuum chambers;

disposing said substrate in said first vacuum chamber;

introducing a first gaseous material into said first vacuum chamber;

applying a first glow discharge to a region in said first vacuum chamber, said first glow discharge depositing a first film on said substrate while maintaining said first gaseous material at sub-atmospheric pressure and while isolating said first vacuum chamber;

transporting said substrate with said first film from said first vacuum chamber into said second vacuum chamber;

introducing a second gaseous material into said second vacuum chamber; and,

applying a second glow discharge to a region in said

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second vacuum chamber, said second glow discharge depositing a second film on said substrate while maintaining said second gaseous material at sub-atmospheric pressure, and while isolating said second vacuum chamber wherein at least one of said first and second gaseous materials and at least one of said films comprises silicon and hydrogen.

11. The method of claim 10 in which one of said first and second gaseous materials in one of said vacuum chambers comprises nitrogen and the other of said first and second gaseous materials is substantially free of said nitrogen from said one of said vacuum chambers.

12. The method of claim 10 in which one of said first and second gaseous materials in one of said vacuum chambers comprises a dopant and the other of said gaseous materials is substantially free of said dopant from said one of said vacuum chambers.

13. The method of claim 10 which includes the steps of: providing a third vacuum chamber;

disposing said substrate in said third vacuum chamber in gas at atmospheric pressure while restricting the flow of said gas at atmospheric pressure between said third vacuum chamber and said first and second vacuum chambers;

evacuating said third vacuum chamber; and,

transporting said substrate from said third vacuum chamber to one of said first and second vacuum chambers while restricting the flow of gases between said first, second and third chambers.

14. The method of claim 13 in which a gas lock restricts the flow of gases between said vacuum chambers.

15. The method of claim 13 in which differential pumping is provided to restrict the flow of gases between said vacuum chambers.

16. The method of claim 14 further comprising:

opening said gas lock; and

transporting said substrate through said gas lock along a path through an evacuable zone between said vacuum chambers while said zone is being evacuated.

17. The method of claim 16 in which a movable arm transports said substrate through said gas lock between said vacuum chambers.

18. The method of claim 10 further comprising the steps of:

providing a third vacuum chamber;

evacuating said third vacuum chamber;

transporting said substrate from said second vacuum chamber to said third vacuum chamber while restricting the flow of gases between said first, second and third vacuum chambers; and,

introducing a gas at atmospheric pressure into said third vacuum chamber while restricting the flow of said gas at atmospheric pressure between said third vacuum chamber and said first and second vacuum chambers.

19. A process for making a film on the surface of a substrate using a gaseous material at sub-atmospheric pressure suitable for sustaining a glow discharge in a vacuum chamber having first and second electrodes juxtaposed in face-to-face spaced relation with said second electrode having an internal cavity and a plurality of apertures formed there through, comprising the steps of:

positioning said electrodes in face-to-face spaced relation; disposing said substrate on said first electrode;

introducing a gaseous material comprising silicon and hydrogen at sub-atmospheric pressure into said internal

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cavity and through said plurality of apertures in said second electrode; and,

maintaining a glow discharge in said gaseous material between said electrodes to form said film on said substrate.

20. A method of making a semiconductor device on a semitransparent substrate having a layer of conducting metal oxide comprising indium comprising the steps of:

providing a vacuum chamber having a first electrode;

disposing said substrate on the surface of said first electrode in said vacuum chamber;

introducing a gaseous material comprising phosphorous at sub-atmospheric pressure into said vacuum chamber;

applying a first glow discharge to a region in said vacuum chamber to fabricate a first film comprising phosphorous on said layer of conducting metal oxide comprising indium on the surface of said substrate;

introducing a second gaseous material comprising silicon and hydrogen at sub-atmospheric pressure into said vacuum chamber; and,

applying a second glow discharge to a region in said vacuum chamber to fabricate a second film comprising silicon and hydrogen on said first film so that a phosphorous-doped ohmic-contact is formed between said films.

21. A method of fabricating a semiconductor device comprising the steps of:

providing a first and second vacuum chambers;

providing an airlock in said first vacuum chamber;

disposing a substrate in said first vacuum chamber in a first gaseous material at atmospheric pressure while said airlock is closed;

evacuating said first and said second vacuum chambers;

transporting said substrate from said first vacuum chamber to said second vacuum chamber;

introducing a second gaseous material comprising silicon and hydrogen into said second vacuum chamber; and,

applying a glow discharge to a region in said second vacuum chamber to said second gaseous material, said glow discharge depositing a film comprising silicon on said substrate while maintaining said second gaseous material at sub-atmospheric pressure, while maintaining said substrate at a temperature and while said airlock is closed.

22. The method of claim 21 in which said film comprising silicon also comprises nitrogen.

23. The method of claim 21 in which said film comprising silicon also comprises phosphorous.

24. The method of claim 21 further comprising the steps of:

projecting an electric field into said region of said second vacuum chamber; and,

controlling said electric field and said pressure of said second gaseous material to position said glow discharge relative to said substrate.

25. The method of claim 21 further comprising the step of:

providing a movable armature for transporting said substrate from said first vacuum chamber through said airlock through a zone to said second vacuum chamber.

26. The method of claim 22 further comprising the step of fabricating an electrical contact to said film comprising silicon and nitrogen to form an insulated gate of a field effect transistor.

27. The method of claim 26 further comprising the step of

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positioning a metal oxide dielectric between said electrical contact and said film comprising silicon and nitrogen.

28. The method of claim 9 in which said films comprising silicon and hydrogen also comprise nitrogen.

29. The method of claim 28 further comprising the step of fabricating an electrical contact to said film comprising silicon, hydrogen and nitrogen to form an insulated gate of a field effect transistor. 5

30. The method of claim 29 further comprising the step of positioning a metal oxide dielectric between said electrical contact and said film comprising silicon, hydrogen and nitrogen. 10

31. The method of producing a semiconductor device comprising the steps of:

providing a first and a second evacuable enclosures; 15

providing a first airlock in said first enclosure;

evacuating said first enclosure;

introducing a first gaseous material comprising silicon in said first enclosure; 20

generating a first glow discharge in said first gaseous material in said first enclosure, said first glow discharge depositing a first film comprising silicon on said substrate while maintaining first gaseous material at sub-atmospheric pressure and while said first airlock is closed; 25

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providing a second airlock in said second enclosure;

evacuating said second enclosure;

transporting said substrate from said first enclosure through a zone outside of said first enclosure into said second enclosure;

positioning said substrate in said second enclosure;

evacuating said second enclosure;

introducing a second gaseous material in said second enclosure; and,

generating a second glow discharge in said second enclosure, said second glow discharge depositing a second film on said first film comprising silicon while maintaining said second gaseous material at subatmospheric pressure and while said second airlock is closed.

32. The method of claim 31 in which said second gaseous material comprises a dopant gas and said first gaseous material comprising silicon is substantially free of said dopant gas.

33. The method of claim 31 in which said second gaseous material comprises nitrogen and said first gaseous material comprising silicon is substantially free of said nitrogen.

34. The method of claim 31 in which said semiconductor device comprises a field effect transistor (FET).

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