US 20150024546A1

(19) **United States**

(12) **Patent Application Publication**

Chang et al.

(10) **Pub. No.: US 2015/0024546 A1**

(43) **Pub. Date: Jan. 22, 2015**

(54) **SYSTEM, STRUCTURE, AND METHOD OF MANUFACTURING A SEMICONDUCTOR SUBSTRATE STACK**

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

(72) Inventors: **Hung-Pin Chang**, Taipei (TW); **Weng-Jin Wu**, Hsin-Chu (TW); **Wen-Chih Chiou**, Zhunan Township (TW); **Chen-Hua Yu**, Hsin-Chu (TW)

(21) Appl. No.: **14/507,467**

(22) Filed: **Oct. 6, 2014**

Related U.S. Application Data

(62) Division of application No. 12/178,021, filed on Jul. 23, 2008, now Pat. No. 8,853,830.

(60) Provisional application No. 61/127,627, filed on May 14, 2008.

Publication Classification

(51) **Int. Cl.**

H01L 21/768 (2006.01)

H01L 25/00 (2006.01)

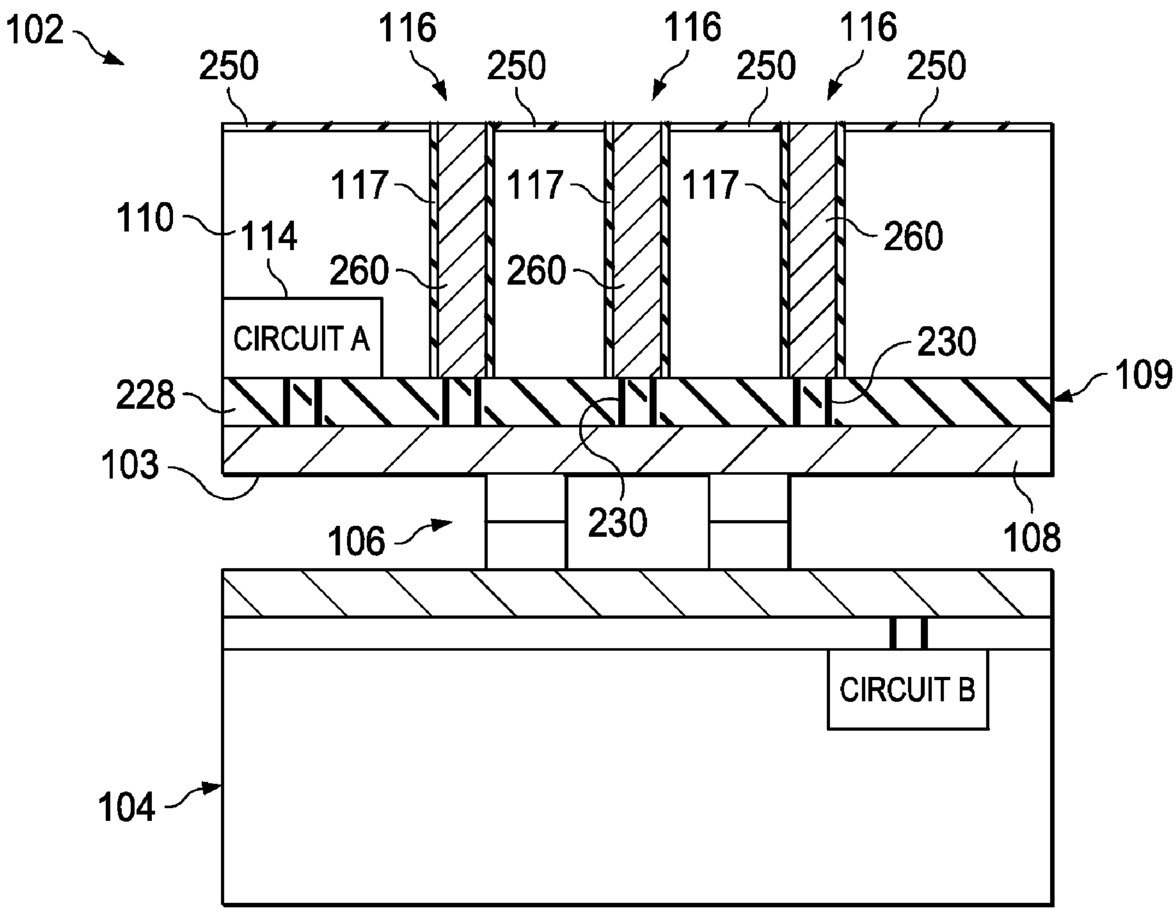
(52) **U.S. Cl.**

CPC ***H01L 21/76898*** (2013.01); ***H01L 21/7684*** (2013.01); ***H01L 21/76877*** (2013.01); ***H01L 21/768*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 2225/06541* (2013.01)

USPC **438/107**; 438/667; 438/618

(57) **ABSTRACT**

A method of manufacturing a semiconductor substrate structure for use in a semiconductor substrate stack system is presented. The method includes a semiconductor substrate which includes a front-face, a backside, a bulk layer, an interconnect layer that includes a plurality of inter-metal dielectric layers sandwiched between conductive layers, a contact layer that is between the bulk layer and the interconnect layer, and a TSV structure commencing between the bulk layer and the contact layer and terminating at the backside of the substrate. The TSV structure is electrically coupled to the interconnect layer and the TSV structure is electrically coupled to a bonding pad on the backside.



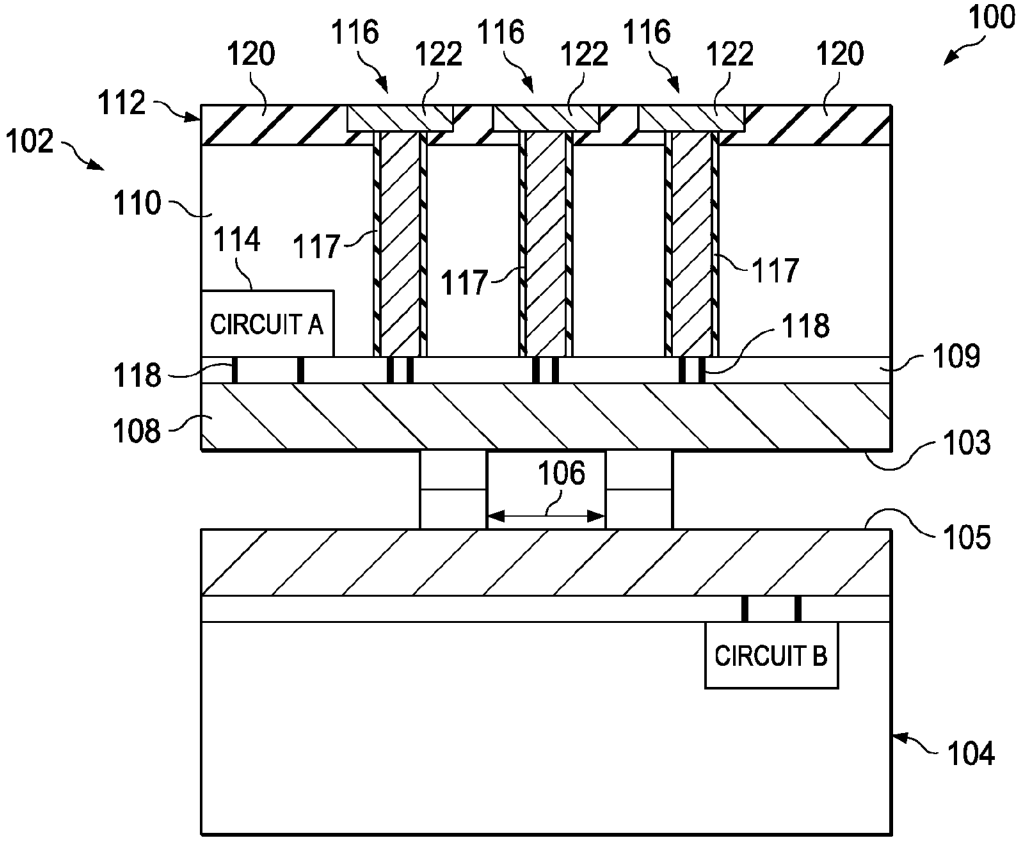

100
102
112
120
116
122
116
122
116
122
120
110
114
117
117
117
CIRCUIT A
118
118
109
108
103
106
105
CIRCUIT B
104

FIG. 1

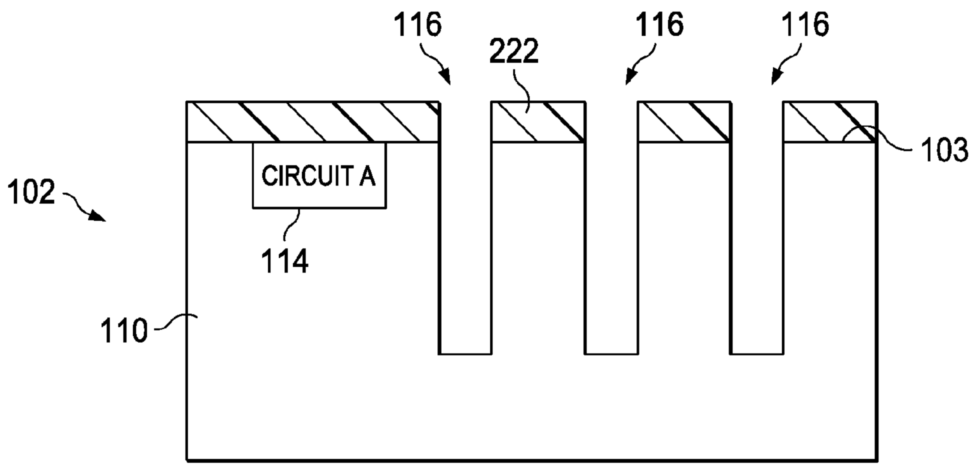

116
222
116
116
103
102
CIRCUIT A
114
110

FIG. 2A

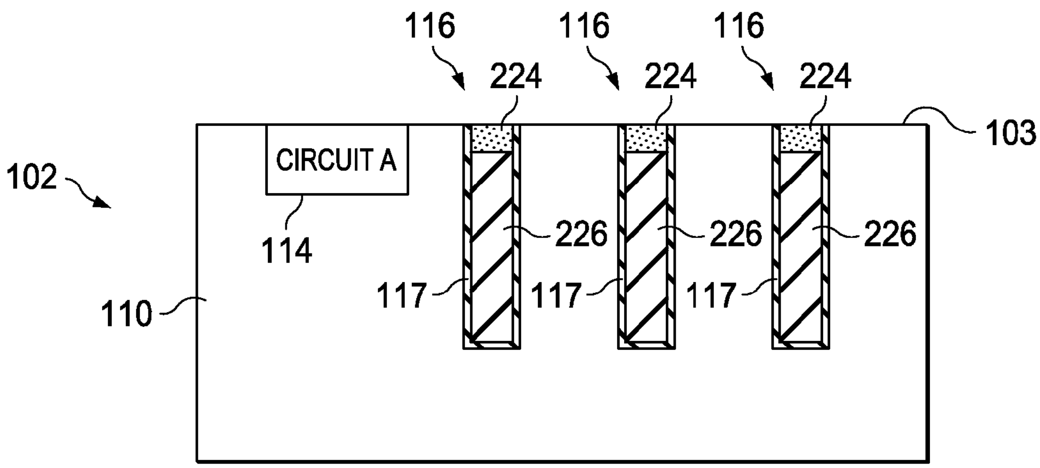

116
116
116
224
224
224
103
102
CIRCUIT A
114
226
226
226
117
117
117
110

FIG. 2B

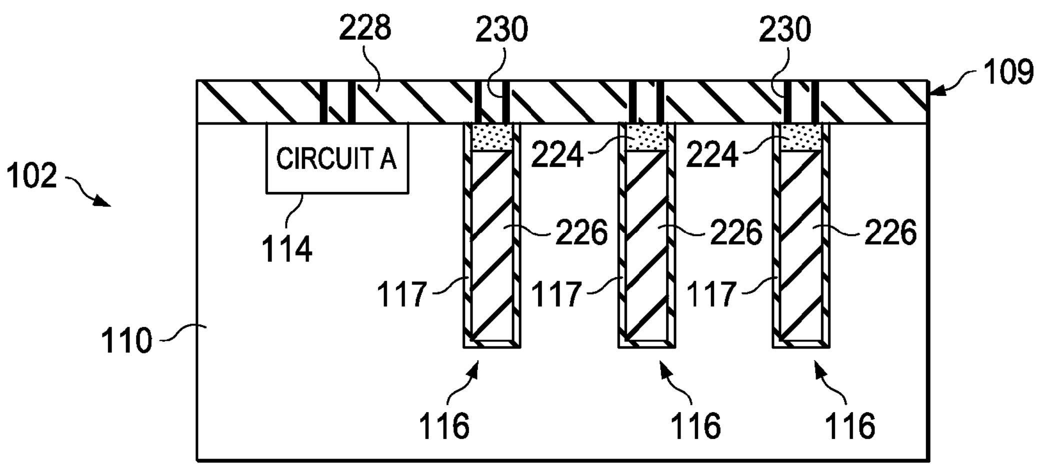

228
230
230
109
102
CIRCUIT A
224
224
114
226
226
226
117
117
117
110
116
116
116

FIG. 2C

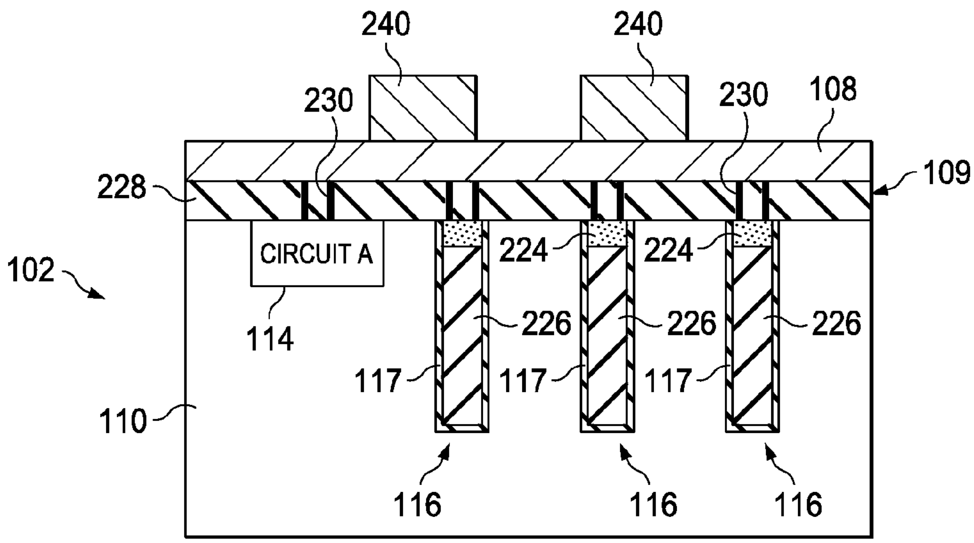

240
240
230
230
108
228
109
CIRCUIT A
224
224
102
114
226
226
226
117
117
117
110
116
116
116

FIG. 2D

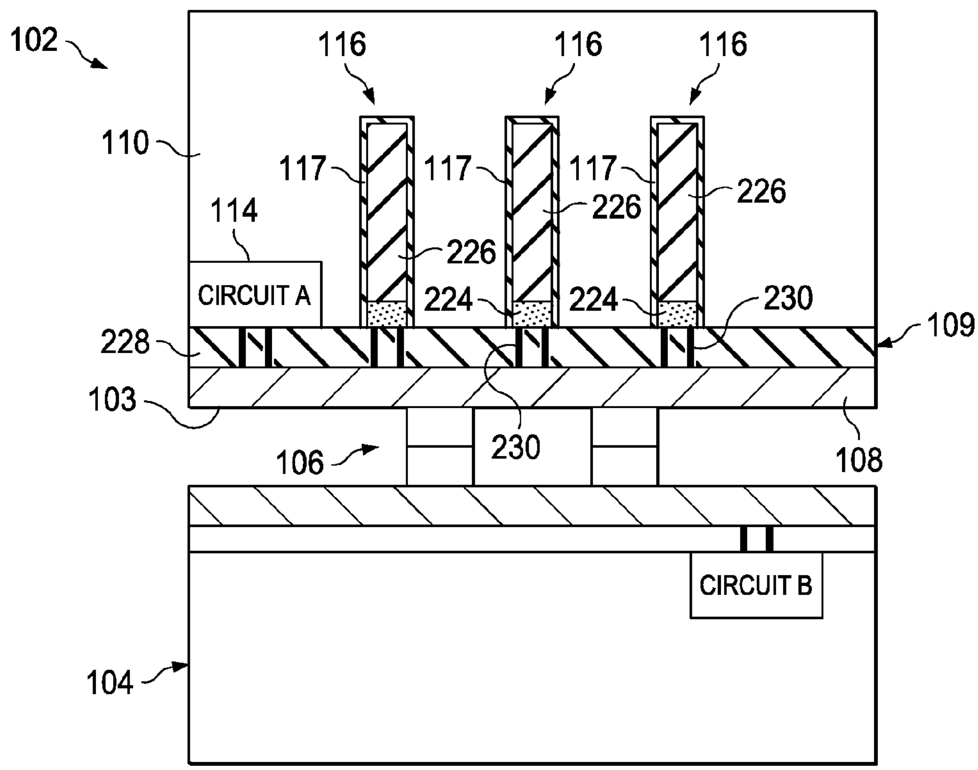

102
116
116
116
110
117
117
117
226
226
114
226
CIRCUIT A
224
224
230
228
109
103
230
106
108
CIRCUIT B
104

FIG. 2E

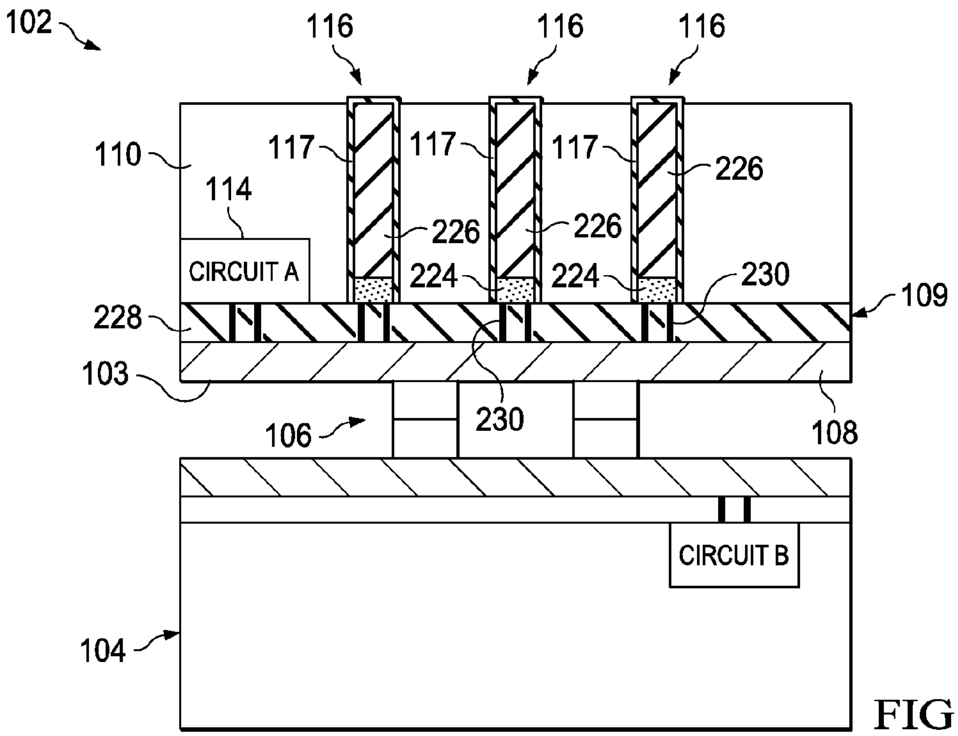

102
116
116
116
110
117
117
117
226
114
226
226
CIRCUIT A
224
224
230
109
228
103
230
108
106
CIRCUIT B
104

FIG. 2F

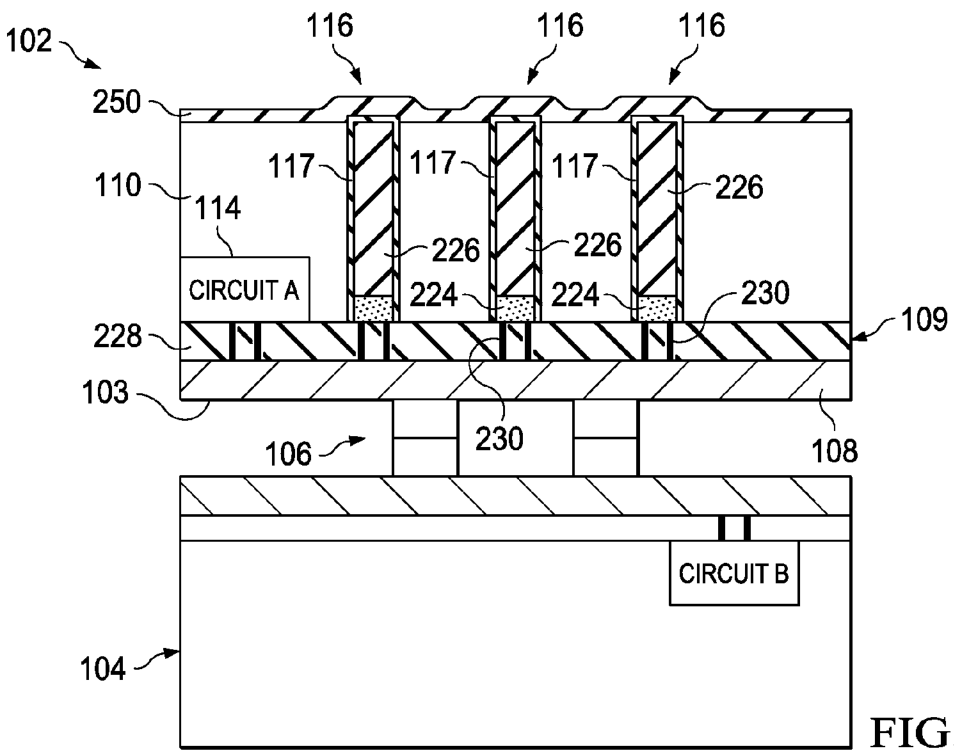

102
116
116
116
250
117
117
117
110
114
226
226
226
CIRCUIT A
224
224
230
109
228
103
230
108
106
CIRCUIT B
104

FIG. 2G

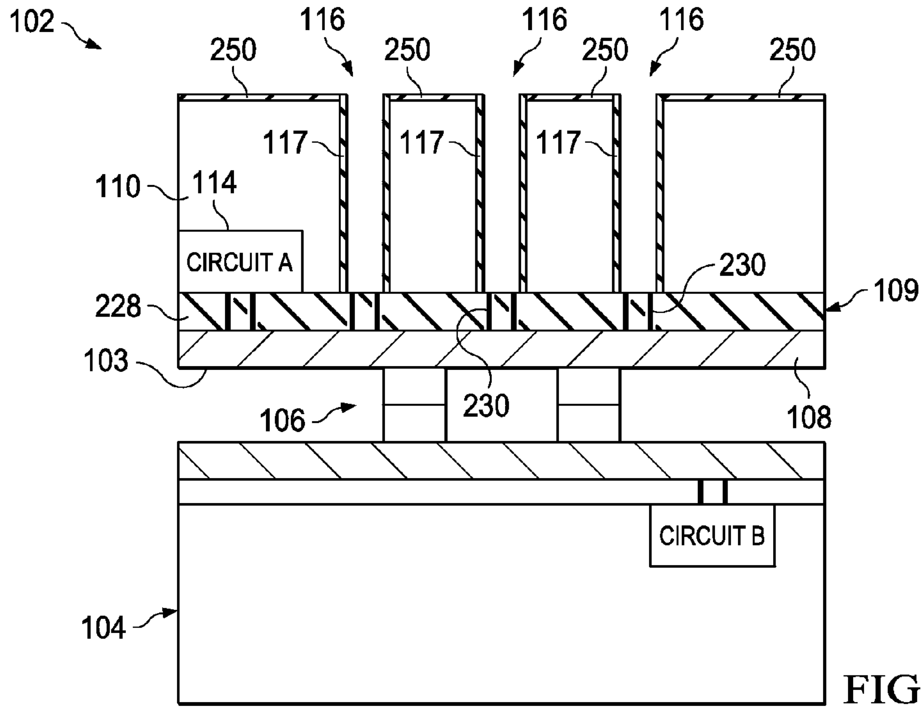

102
116
116
116
250
250
250
250
117
117
117
110
114
CIRCUIT A
230
109
228
103
230
108
106
CIRCUIT B
104

FIG. 2H

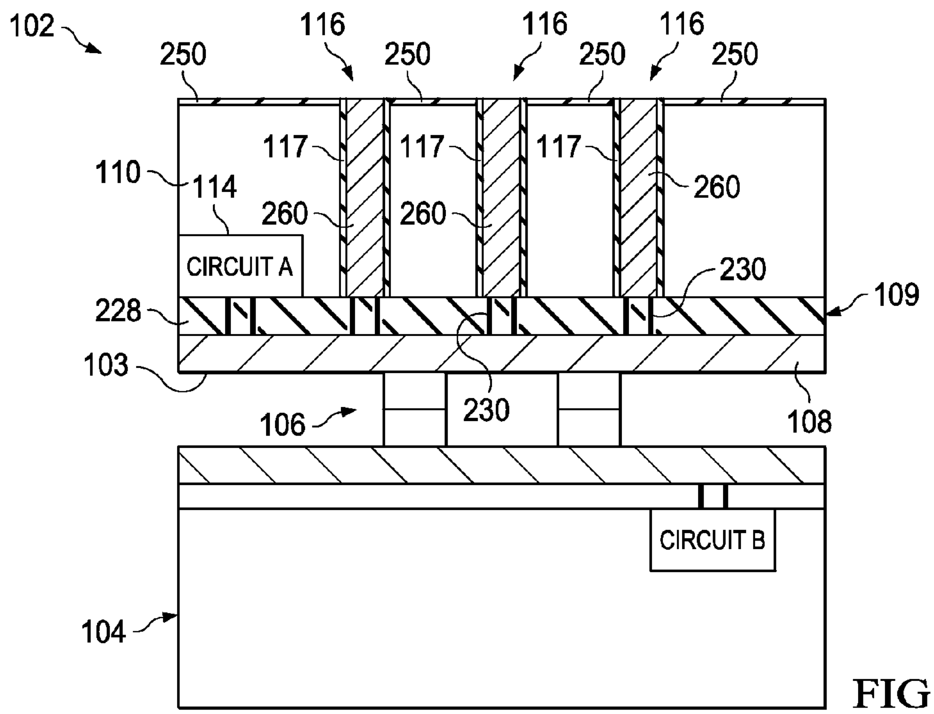

102
116
116
116
250
250
250
250
117
117
117
110
114
260
260
260
CIRCUIT A
230
109
228
103
230
108
106
CIRCUIT B
104

FIG. 2I

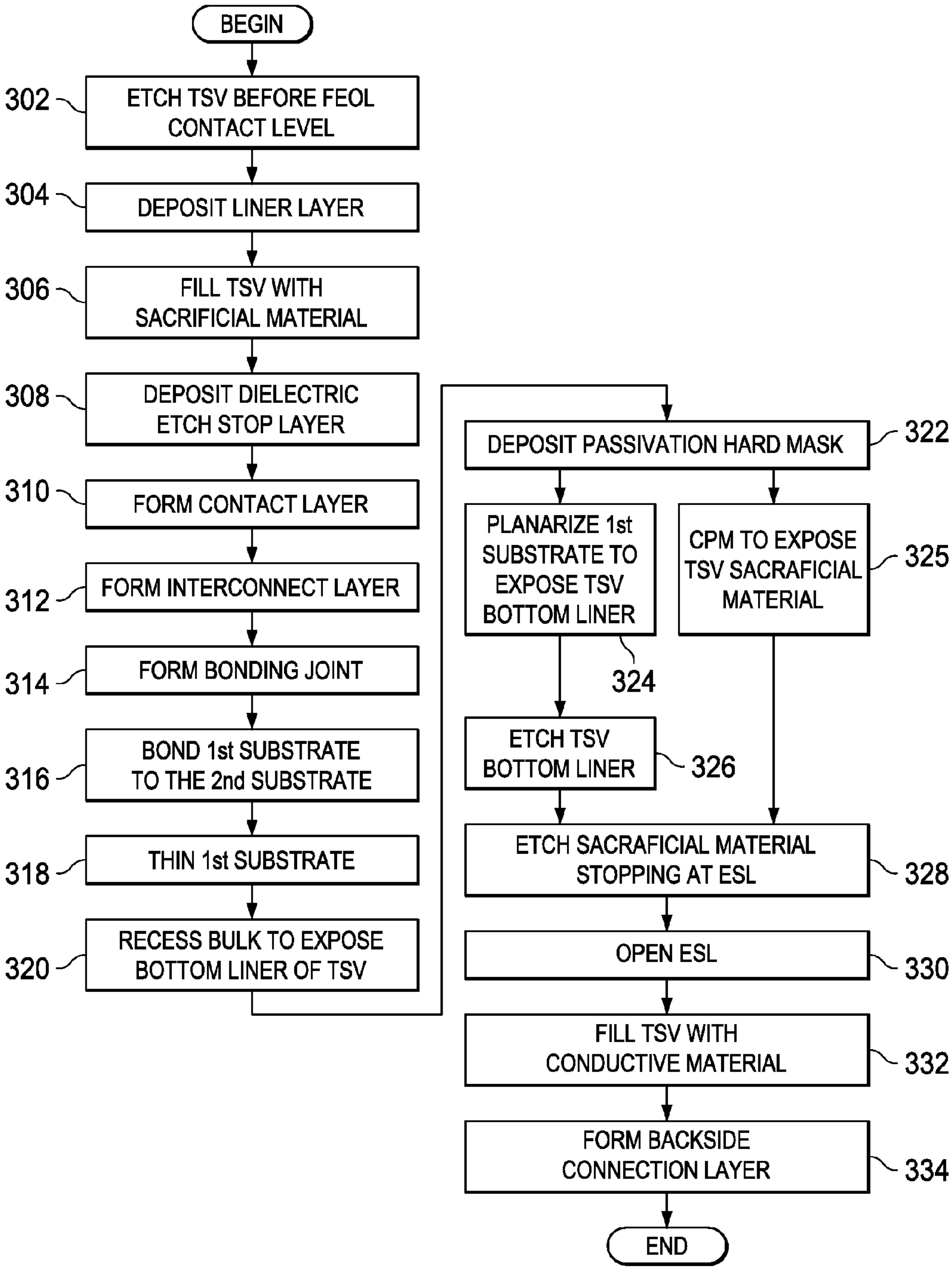

BEGIN
302
ETCH TSV BEFORE FEOL CONTACT LEVEL
304
DEPOSIT LINER LAYER
306
FILL TSV WITH SACRIFICIAL MATERIAL
308
DEPOSIT DIELECTRIC ETCH STOP LAYER
310
FORM CONTACT LAYER
312
FORM INTERCONNECT LAYER
314
FORM BONDING JOINT
316
BOND 1st SUBSTRATE TO THE 2nd SUBSTRATE
318
THIN 1st SUBSTRATE
320
RECESS BULK TO EXPOSE BOTTOM LINER OF TSV
DEPOSIT PASSIVATION HARD MASK
322
PLANARIZE 1st SUBSTRATE TO EXPOSE TSV BOTTOM LINER
324
CPM TO EXPOSE TSV SACRAFICIAL MATERIAL
325
ETCH TSV BOTTOM LINER
326
ETCH SACRAFICIAL MATERIAL STOPPING AT ESL
328
OPEN ESL
330
FILL TSV WITH CONDUCTIVE MATERIAL
332
FORM BACKSIDE CONNECTION LAYER
334
END

FIG. 3

[0013] FIG. **1** is a cross sectional depiction of a semiconductor substrate stacking system, in accordance with an illustrative embodiment;

[0014] FIGS. **2**A-**2**I are cross sectional depictions of a semiconductor substrate stacking system during selected process steps of an illustrative embodiment; and

[0015] FIG. **3** is a flow chart of a method of forming a semiconductor substrate stacking system.

[0016] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0017] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that an illustrative embodiment provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0018] The present invention will be described with respect to illustrative embodiments in a specific context, namely a front-to-front stacked semiconductor substrate system. The invention may also be applied, however, to other semiconductor substrate systems, such as single substrates, back-to-back bonded substrates, chip stacks, multiple substrate stacks, and the like. Embodiments may also have application in other through substrate via processes.

[0019] With reference now to FIG. **1**, a system for stacking semiconductor substrates is shown. The term "substrate" herein, generally refers to a semiconductor substrate including a bulk layer **110** on which various layers and structures are formed. Silicon may be used or compound semiconductors, GaAs, InP, Si/Ge, or SiC, as examples, may be used in place of silicon. Example layers may include such layers as dielectric layers, doped layers and polysilicon layers. Example structures may include transistors, resistors, and/or capacitors, which may or may not be interconnected through an interconnect layer to additional active circuits.

[0020] System **100** shows substrate-A **102** inverted and bonded to substrate-B **104** at bonding joint **106**. In an embodiment shown, front-face-A **103** of substrate-A **102** is bonded to front-face-B **105** of substrate-B **104** at bonding joint **106**. Substrate-A **102** comprises interconnect layer **108**, contact layer **109**, bulk layer **110**, and backside connection layer **112**. Circuit-A **114** is also shown. Circuit-A **114** may extend from the upper layers of bulk layer **110** through contact layer **109** to interconnect layer **108**.

[0021] Through substrate via (TSV) structures **116** are shown in substrate-A **102** and not in substrate-B **104**. However, substrate-B **104** may have TSV structures in another embodiment. In yet another embodiment, multiple substrates may be stacked one on the other in front-to-front, front-to-back, and back-to-back configurations. TSV structures **116** may have lining **117** comprising a dielectric such as an oxide, nitride, or the like. TSV structures **116** are filled with a conductive material such as Al, Cu, other metals, alloys, doped polysilicon, combinations, and the like. Preferably, TSV structures **116** are filled with metal.

[0022] Semiconductor circuits, such as circuit-A **114**, are manufactured by forming active regions in a bulk layer, such as bulk layer **110**, depositing various insulating, conductive, and semiconductive layers over the substrate, and patterning them in sequential steps. The interconnect layer typically provides connections to underlying active regions and connections within and over the substrate. The interconnect layer includes one or more layers of metal interconnect having the conductive lines disposed within an insulating material. A contact layer, such as contact layer **109** is comprised of conductors disposed in dielectrics, which connect components in bulk layer **110** of substrate-A **114** to interconnect layer **108**. The conductors in the contact layer may be any conducting material such as doped polysilicon, Al, Cu, W, alloys, combinations, and the like. Preferably, the contact material is W. Dielectrics in the contact layer may be oxides, nitrides, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), fluorinated silicate glass or fluorinated silicon oxide glass (FSG) or any electrically isolating materials.

[0023] TSV structures **116** are etched prior to contact layer **109** of circuit-A **114**. Contacts **118** provide electrical coupling between the TSV structures **116** and interconnect layer **108**. Backside connection layer **112** provides electrical interconnection between substrate-A **102** and outside systems, which may include other stacked substrates. Through bonding joint **106** backside connection layer **112** may also provide electrical interconnection between substrate-B **104** and outside systems. Backside connection layer **112** is comprised of a backside dielectric **120** and backside metal **122**. Backside dielectric **120** may be, for example, a layer of SiN and a layer of an undoped silicon oxide glass (USG), or the like.

[0024] FIGS. **2**A-**2**I are cross sectional depictions of a semiconductor substrate stacking system during selected process steps of an illustrative embodiment.

[0025] FIG. **2**A shows substrate-A **102** with front-face **103** oriented up, as may be typical during circuit processing, and with TSV structures **116** oriented down into bulk layer **110** (note that substrate-A is shown oriented "flipped" relative to FIG. **1**). Circuit-A **114** is shown prior to contact etch.

[0026] Bulk layer **110** may be patterned, for example, by depositing a photoresist **222** over the top surface of bulk layer **110**. Using a reticle, having transparent regions and opaque regions, photoresist **222** or a hard mask may be patterned using techniques well known in the art. In an embodiment implementing a hard mask, the resulting TSV structure may then terminate substantially the thickness of the hard mask above the substrate, rather than substantially at the substrate. The TSV structures may be etched using a reactive-ion plasma process for example. A Bosch process, which is capable of achieving high aspect ratio structure, may be implemented in an embodiment. In an alternate embodiment a wet etch may be implemented. The TSV structures may range in depth from tens to hundreds of microns.

[0027] TSV structures **116**, thus etched, are coated with a dielectric layer, such as SiO_2 or SiN to form liner **117**, as shown in FIG. **2**B. Liner **117** may be comprised of oxides, nitrides, combinations, or other dielectrics. Preferably, the liner is SiO_2, formed in a wet oxidation process.

[0028] Liner **117** may act as a passivation layer between bulk layer **110** and the subsequent metal conductor filled into TSV structures **116**. An advantage of an illustrative embodiment is that high quality dielectrics may be more readily used in this step of the substrate processing.

[0029] TSV structures **116** are then filled with sacrificial material **226**. The sacrificial material may be a nitride, an oxide, a doped or undoped polysilicon, or the like. One consideration of the choice of sacrificial material may be a high etch selectivity between liner **117** and subsequently deposited etch stop layer (ESL) **224**. In the illustrative embodiment shown, undoped polysilicon is used to fill into the TSV structure. After deposition, a planarization process may be performed to remove any undoped polysilicon formed outside of the TSV structure.

[0030] TSV structures **116** are then capped with a dielectric layer, which acts as an ESL **224** during the subsequent etch of sacrificial material **226** (described in FIG. **2**H). ESL **224** may comprise oxide, nitride, other dielectrics, combinations, or the like. ESL **224** is preferably SiO_2. One consideration of the choice of ESL material may be a high etch selectivity between the ESL material and liner **117** plus the subsequently deposited hard mask (described further in FIG. **2**G).

[0031] Turning to FIG. **2**C, an insulating material layer **228** is then disposed on bulk layer **110**. Insulating material layer **228** may be, for example, SiON, SiN, PSG, combinations, or the like. Insulating material layer **228** may be patterned and openings for contacts **230** may be etched. Contacts **230** may be comprised of metal, such as W, Al, Cu, combinations, or the like, filling the contact openings. Alternatively, contacts **230** may be formed of doped polysilicon or other sufficiently conductive material. Contacts **230** are formed in insulating material layer **228**. Contact layer **109** comprises insulating material layer **228** and contacts **230**. Note that some contacts **230** found in contact layer **109** may contact the TSV structures **116** and other contacts **230** found in contact layer **109** may contact circuit-A **114**.

[0032] Turning now to FIG. **2**D, interconnect layer **108** is shown. A single substrate may contain many active regions and/or functioning circuits. For example, bulk layer **110** may include one or more semiconductor elements, e.g. transistors, diodes, etc. (not shown) and circuit-A **114**. Bulk layer **110** may also include other active components or circuits formed therein. At times, it is necessary to connect one circuit or device with another circuit or device that is not immediately adjacent to it. An interconnect layer, such as interconnect layer **108** may be used for this purpose.

[0033] Interconnect layer **108** may be comprised of a series of inter-metal dielectric (IMD) and conductive lines interconnected by vias (not shown). Interconnect layer **108** is further comprised of metal and inter-metal dielectrics, formed by disposing alternate layers of metal and inter-metal dielectrics. Conductive lines may comprise Cu, Al, W, other conductive material, or combinations thereof, as examples. One or more barrier layers and seed layers may be deposited prior to the deposition of the Cu, Al, W, other conductors, or combinations thereof, for example (not shown). The conductive lines may be disposed employing a damascene process, a dual damascene process, an etched conductive layer process, or the like. Different layers of the multilayered interconnect layer **108** may be comprised of different materials. Top metal **240** is formed for bonding substrate-A **102** to another substrate, or system. For example, top metal **240** may employed for use as a bonding joint, such as bonding joint **106**, in FIG. **1**. Top metal **240** may comprise Cu, Al, other metals, combinations, other conductors, and the like.

[0034] The insulating layers or inter-metal dielectrics described herein may comprise traditional insulating materials used for interconnect layers such as SiO_2, or alternatively may comprise low-κ materials. The low-κ material may comprise diamond-like carbon, such as Black Diamond™ by Applied Materials, Inc., phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), fluorinated silicate glass or fluorinated silicon oxide glass (FSG), SiO_xC_y, Spin-On-Glass, Spin-On-Polymers, SILK™ by Dow Chemical, FLARE™ by Honeywell, LKD (low-κ dielectric) from JSR Micro, Inc., hydrogenated oxidized silicon carbon material (SiCOH), amorphous hydrogenated silicon (a-Si:H), SiO_xN_y, SiC, SiCO, SiCH, compounds thereof, composites thereof, and/or combinations thereof, as examples. In other applications, the insulating layers **218** may comprise a high dielectric constant material, having a dielectric constant of greater than about 4.0, for example. The insulating layers **218** may alternatively comprise a combination of one or more low-κ materials, high-κ material, SiO_2, SiN, or combinations, for example.

[0035] There may be one, or a plurality of metallization layers included in interconnect layer **108**, for example (not shown).

[0036] FIG. **2**E shows substrate-A **102** inverted and bonded to second substrate-B **104** employing bonding joint **106**. Substrate-B **104** may be a second wafer, a second chip, a routing substrate, or the like.

[0037] After bonding to substrate-B **104**, substrate-A **102** is thinned. The wafer may be thinned in a grinding, lapping, or polishing process. The wafer may be thinned to a range of several tens of microns, thus removing a portion of bulk layer **110**.

[0038] Turning to FIG. **2**F, the bulk layer **110** on the backside of substrate-A **102** is shown recessed to expose the bottom of liner **117**. The recess process may be performed in a two-step process by, for example, a first CMP process and a second wet etch process. Alternatively, substrate **102** may be thinned and the backside of substrate-A **102** recessed in a single process step. The recess process may have a high etch selectivity between bulk layer **110** and liner **117**.

[0039] Turning to FIG. **2**G, passivation dielectric layer **250** is disposed. The passivation dielectric layer **250** serves as the hard mask for removing sacrificial material **226** from TSV structures **116** and serves as the passivation layer for the subsequent conductive material disposed in TSV structures **116**. Passivation dielectric layer **250** may be a plasma enhanced USG material or other dielectric material.

[0040] The backside of substrate-A **102** is then planarized (again recall that the backside of substrate **102** is oriented up). A CMP process may be used for the planarization step. The CMP process may stop on liner **117**, before exposing sacrificial material **226**. A second wet or dry etch may be employed to expose sacrificial material **226**. Alternatively sacrificial material **226** may be exposed in a one-step CMP or etch process. The etch of sacrificial material **226** may be implemented by a dry or wet method with the high selectivity between the sacrificial material **226** and the passivation dielectric layer **250**.

[0041] The underlying bulk material is protected from the sacrificial material **226** etch by the passivation dielectric layer **250**, which acts as a hard mask. Sacrificial material **226** etch stops at ESL **224**. Next, ESL **224** is etched, exposing contact **230** for electrical interconnection.

[0042] As noted earlier the passivation dielectric layer **250** and the ESL material may be selected to have a high etch selectivity. Removal of ESL **224** allows access to contacts

230, which in turn electrically couples the TSV structures **116** to interconnect layer **108**. The resulting structure is shown in FIG. **2**H.

[0043] Turning to FIG. **2**I, the TSV structures **116** are filled with conducting material **260**. Metal, such as Al, Cu, alloys and the like may be sputtered, electro-plated, or screen-printed to fill TSV structures **116**. Alternatively, other conductive materials may be used. Following the disposition of conducting material **260**, substrate **102** may again be planarized by a CMP process.

[0044] The process is then completed by forming backside connection layer **112**, as shown in FIG. **1**. Backside connection layer **112** is comprised of a dielectric layer. For example, the dielectric layer may be formed by a SiN deposition, followed by a USG deposition. The dielectric layer may be patterned and etched. Backside metal **122** is formed by, for example, a damascene process or a patterning of a metal layer. Backside connection layer **112** may be comprised therefore of the SiN/USG dielectric layer and the backside metal **122**. The substrate may then be bonded to further outside systems, using methods well known in the art. The resultant structure is shown in FIG. **1**.

[0045] FIG. **3** is a flow chart of a method of forming a substrate within a semiconductor substrate stacking system. The process begins by etching TSV openings before the front end of line (FEOL) contact level (step **302**) on a first substrate. The etched TSV is coated with a liner (step **304**). The liner may act as a passivation layer providing a barrier between the substrate and the eventual conductive material in the finished TSV structure. The liner may be any dielectric, for example, a silicon nitride, a silicon oxide, or the like. An advantage of an illustrative embodiment is the quality of the dielectric that may be used for the liner at the pre-contact stage of processing. A high quality oxide may be used since no metals have been incorporated thus far in the process.

[0046] The TSV structure is then filled with a sacrificial material (step **306**), forming a temporary plug in the TSV structure. The sacrificial material may be polysilicon, a dielectric, a polymer, any combination of these materials, or the like. A consideration in selecting a sacrificial material may be how the temporary material will be removed. A high selectivity between the sacrificial material and the subsequent hard mask may be desirable.

[0047] Following step **306**, filling the TSV structure with sacrificial material, a dielectric etch stop layer (ESL) is disposed on top of the sacrificial material (step **308**). The etch stop layer may be an oxide, nitride, other suitable dielectric, or the like. Following the ESL, the contact layer is formed (step **310**). The contact layer comprises a dielectric layer or combination of dielectric layers, such as SiON, SiN, PSG and the like, and metal or conductive contacts, which may be W, Al, Cu, doped polysilicon, or the like.

[0048] Next, the interconnect layer is formed (step **312**). The interconnect layer may be formed of Cu, Al, other metals, alloys, or conductive material combinations, sandwiched between inter-metal dielectric layers, which may be composed of FSG, USG, or the like. A top metal layer is formed which may be employed as a bonding joint (step **314**).

[0049] The first substrate may then be inverted and bonded to a second substrate (step **316**). In another embodiment, the second substrate may also have a TSV structure or structures and be stacked on a third substrate. In yet another embodiment, the first substrate may continue processing without bonding to another substrate.

[0050] The first substrate is then thinned (step **318**). The thinning process may be done by mechanical cutting, wet or dry etching process.

[0051] The bulk material between the TSV structures is then recessed (step **320**) to reveal the TSV structure liner (as shown in FIG. **2**F). A hard mask is deposited (step **322**) on the backside of the first substrate, covering the exposed TSV structure liner. The hard mask may be a dielectric and may be, for example, a plasma-enhanced USG. In addition to serving as a hard mask during the TSV structure sacrificial material removal, the hard mask serves as the passivation layer for the eventual TSV structure metal filling process.

[0052] The hard mask layer, disposed on the backside of the first substrate, is then planarized. The planarization may consist of, for example, a CMP process, which stops upon exposure of the liner (step **324**). The planarized backside is then blanket etched to remove the exposed portion of the liner (step **326**). Further, the blanket etch process may be a wet or dry etch. Alternatively, the CMP process may be extended to remove the exposed liner in one step (step **325**). In either process, the sacrificial material in the TSV structure is exposed. A dry or wet etch may be used to remove the sacrificial material (**328**). The sacrificial material etch stops at the ESL layer. As noted above, a high selectivity between the hard mask and the ESL material may be desired.

[0053] The ESL is then etched (step **330**), using either a wet or dry etch, as suitable. In an illustrative embodiment an anisotropic dry etch is implemented to limit the etch effect on liner **117**.

[0054] The TSV structure is then filled with conductive material (step **332**), for example, metals, metal alloys and the like. The filling process may be a sputter process, electroplating process, a screen printing process, or the like. The metal surface of the backside of the first substrate is then planarized. A layer of SiN may be deposited followed by a dielectric layer of, for example, USG. The backside of the first substrate is then patterned and etched, to form openings or trenches to receive a further disposal of metal for the backside metal structures, thus forming backside connection layer (step **334**). The substrate may be processed further with processes well known by those of ordinary skill in the art or the process may then end.

[0055] Although the illustrative embodiment and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, many of the features and functions discussed above can be implemented in software, hardware, or firmware, or a combination thereof. As another example, it will be readily understood by those skilled in the art that layer compositions may be varied while remaining within the scope of the present invention.

[0056] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods, and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention.

Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A method comprising:

etching a front-face of a first substrate to create a through substrate via (TSV), at a step before contact etch;

forming at least a first contact between the TSV and an interconnect layer;

forming at least a second contact between an active region and the interconnect layer;

thinning a backside of the first substrate to expose the TSV;

filling the TSV with a conductive material; and

disposing a backside bonding pad, wherein the backside bonding pad is electrically coupled to the TSV.

2. The method of claim **1** further comprising:

lining the TSV with a dielectric.

3. The method of claim **2**, wherein the dielectric is disposed into the TSV prior to any metal processes performed on the first substrate.

4. The method of claim **1** further comprising:

filling the TSV with a sacrificial material, before forming the at least first contact.

5. The method of claim **4**, wherein the sacrificial material is selected from the group consisting of a nitride, an oxide, a doped polysilicon or an undoped polysilicon.

6. The method of claim **4** further comprising:

depositing an etch stop layer on the sacrificial material in the TSV, before forming the at least first contact.

7. The method of claim **6** further comprising:

disposing a hard mask passivation layer on the backside of the first substrate, following thinning the backside;

planarizing the backside of the first substrate to expose the sacrificial material;

removing the sacrificial material; and

removing the etch stop layer prior to filling the TSV with the conductive material.

8. The method of claim **7**, wherein an etch selectivity for the etch stop layer is greater than an etch selectivity of the hard mask passivation layer.

9. The method of claim **1**, wherein the at least first contact is an array of first contacts contacting a single TSV.

10. The method of claim **1** further comprising:

following filling the TSV with the conductive material, disposing a dielectric topping layer on the backside of the first substrate.

11. The method of claim **1** further comprising:

after the forming at least the second contact between the active region and the interconnect layer, electrically coupling a first bonding joint to the interconnect layer; and

physically bonding the first bonding joint to a second bonding joint on a second substrate, before thinning the backside of the first substrate to expose the TSV.

12. A method comprising:

etching a recess in a first side of a first substrate, the recess extending partially into the first substrate, the recess adjacent an active region in the first side of the first substrate;

lining the recess with a dielectric material;

filling the recess with a first material;

forming contacts over the first side of the substrate with at least one contact coupled to the active region and at least another contact aligned with the first material in the recess;

forming an interconnect layer over the contacts and coupled to the at least one contact and the at least another contact;

forming a bond pad over the interconnect layer;

thinning a second side of the substrate to expose the dielectric material;

removing the first material from the recess; and

filling the recess with a conductive material, the conductive material in the recess being coupled to the at least another contact.

13. The method of claim **12**, wherein the removing the first material from the recess removes substantially all of the first material from the recess and leaves the dielectric material lining the recess.

14. The method of claim **12**, wherein filing the recess with a first material further comprises:

forming an etch stop layer in the recess, the etch stop layer being formed of a material selected from a group of materials consisting of Si, Si_xC_y, Si_xN_y, Si_xC_y, Si_xO_y, $Si_xO_yN_z$; and

forming a second layer over the etch stop layer in the recess, the second layer being formed of a material selected from a group of materials consisting of a nitride, an oxide, a doped polysilicon, or an undoped polysilicon.

15. The method of claim **14**, wherein the removing the first material from the recess further comprises:

performing a first etch process to remove the second layer from the recess, the first etch process exposing the etch stop layer; and

performing a second etch process to remove the etch stop layer from the recess, the second etch process exposing the at least another contact.

16. The method of claim **12**, wherein the at least another contact comprises a plurality of conductive contacts contacting the conductive material in the recess.

17. The method of claim **12**, wherein the removing the first material from the recess further comprises:

forming a passivation layer over the second side of the substrate and the exposed dielectric material lining the recess;

planarizing the passivation layer and the dielectric material to expose the first material in the recess; and

selectively etching the first material from the recess.

18. A method comprising:

forming an active region in a first surface of a first substrate;

etching a recess from the first surface of the first substrate into the first substrate;

lining the recess with a dielectric material;

filling the recess with a sacrificial material, the sacrificial material having a different material composition than dielectric material;

forming contacts over the first surface of the first substrate, a first contact being coupled to the active region and a second contact over and aligned with the sacrificial material;

forming an interconnect layer over and coupled to the first and second contacts;

forming a bond pad over the interconnect layer, the bond pad being coupled to at least one of the first contact and the second contact;

bonding the first substrate to a second substrate using the bond pad;

thinning the first substrate from a second surface of the first substrate, the second surface being opposite the first surface, the thinning step exposing a portion of the dielectric material lining the recess;

removing the sacrificial material from the recess from the second surface of the first substrate; and

filling the recess with a conductive material to form a through substrate via (TSV) in the first substrate, the second contact being directly coupled to the conductive material of the TSV.

19. The method of claim **18**, wherein the removing the sacrificial material from the recess from the second surface of the first substrate removes substantially all of the sacrificial material from the recess and leaves the dielectric material lining the recess.

20. The method of claim **18**, wherein the first contact comprises a plurality of conductive contacts contacting the active region, and the second contact comprises a plurality of conductive contacts contacting the conductive material of the TSV.

* * * * *