(12) **United States Patent**
Huang et al.

(10) **Patent No.: US 6,790,765 B1**

(45) **Date of Patent: Sep. 14, 2004**

(54) **METHOD FOR FORMING CONTACT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/720,275**

(22) Filed: **Nov. 25, 2003**

(51) **Int. Cl.**[7] **H01L 21/4763**

(52) **U.S. Cl.** **438/622**; 438/258; 438/637

(58) **Field of Search** 438/622, 257, 438/258, 637, 638, 639, 620, 621

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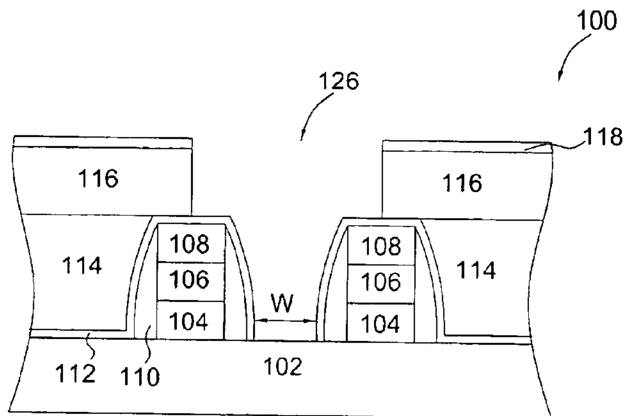
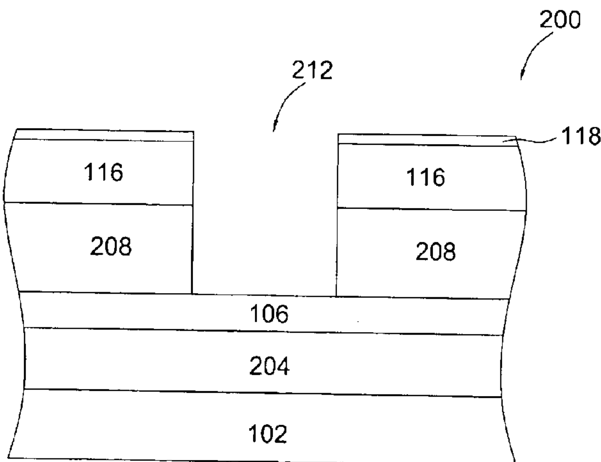
(57) **ABSTRACT**

A method for forming contacts on a semiconductor device is provided. The method includes steps of forming an opening on a gate contact area, depositing a dielectric layer on a bit-line contact area and the opening, coating a photoresist to etch the dielectric layer, removing the photoresist and finally forming a conductive layer on a bit-line contact opening and a gate contact opening.

14 Claims, 9 Drawing Sheets





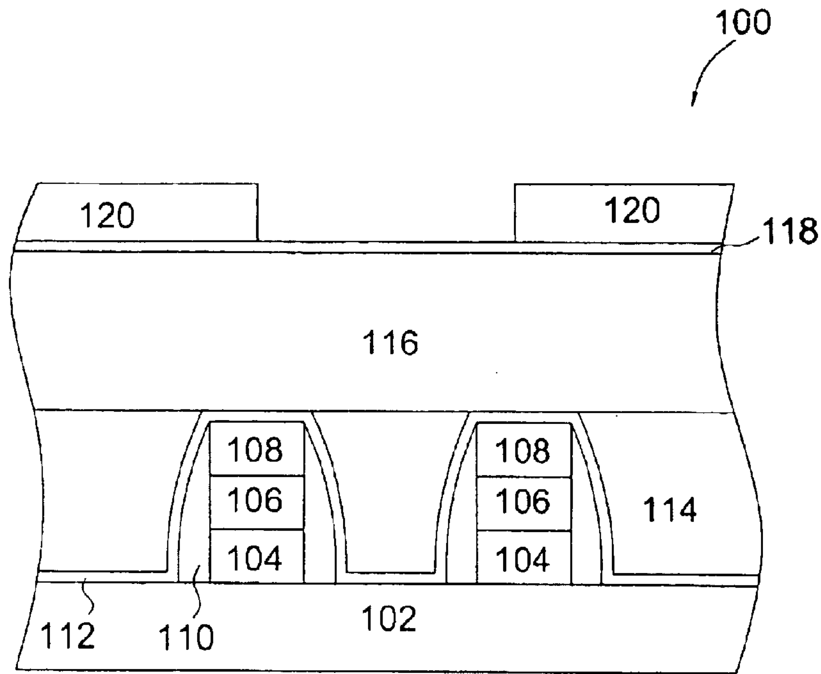


Fig.1A(prior art)

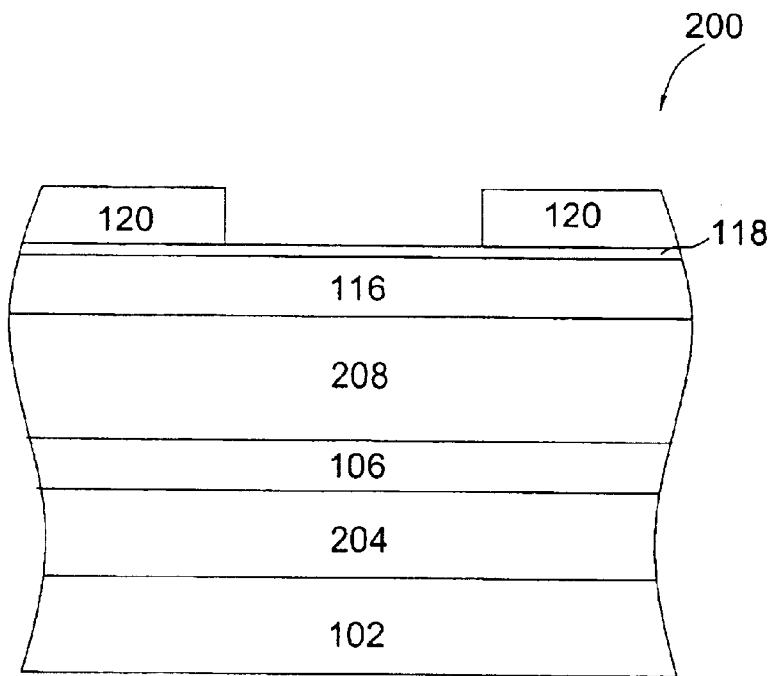


Fig.1B(prior art)

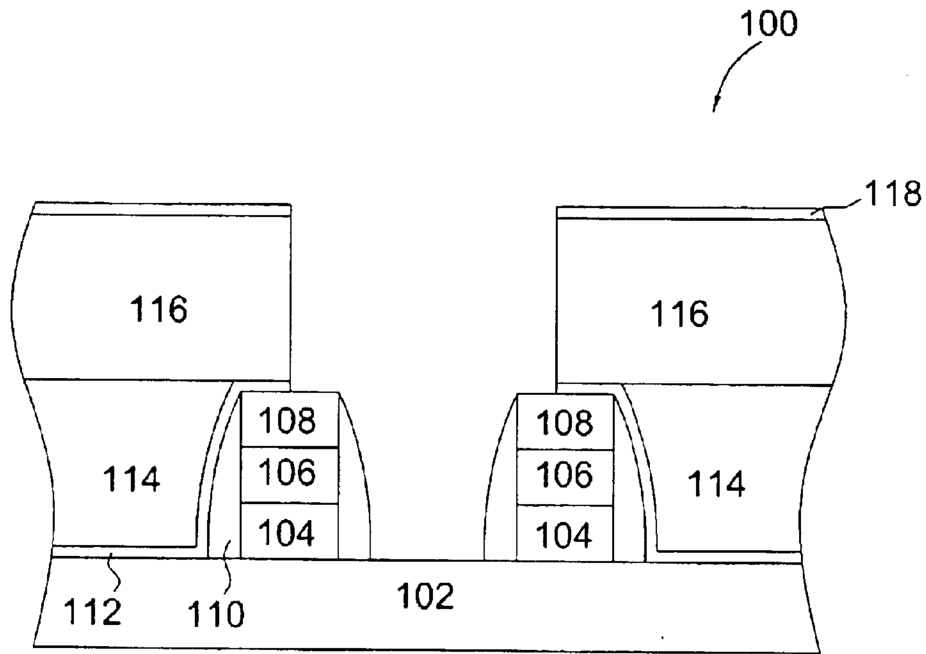


Fig.2A(prior art)

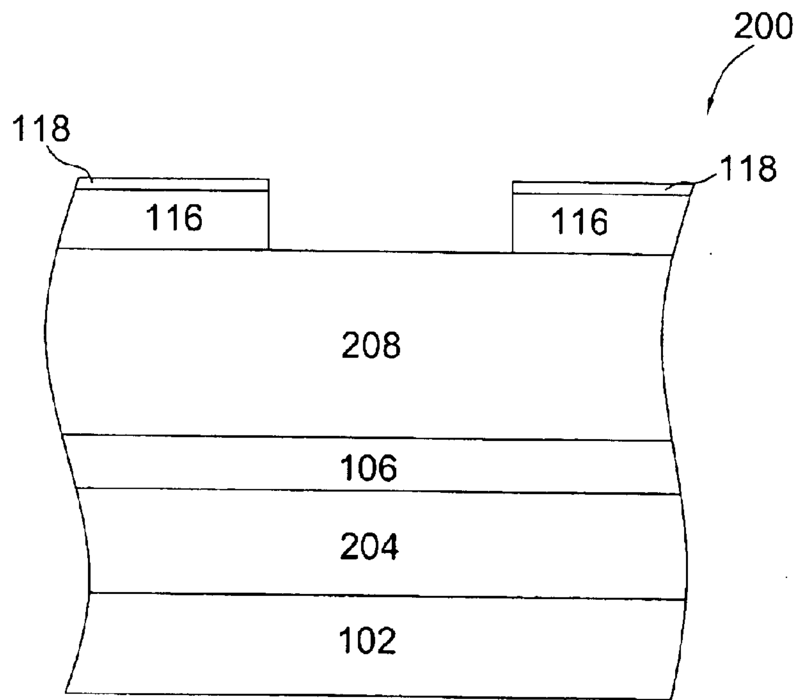


Fig.2B(prior art)

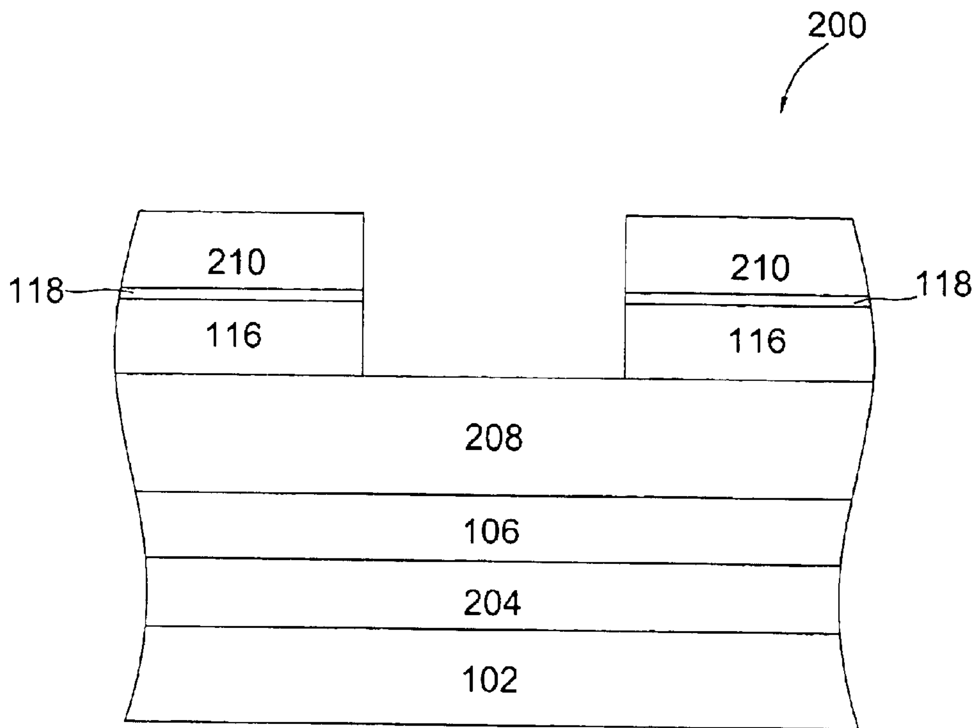


Fig.3A(prior art)

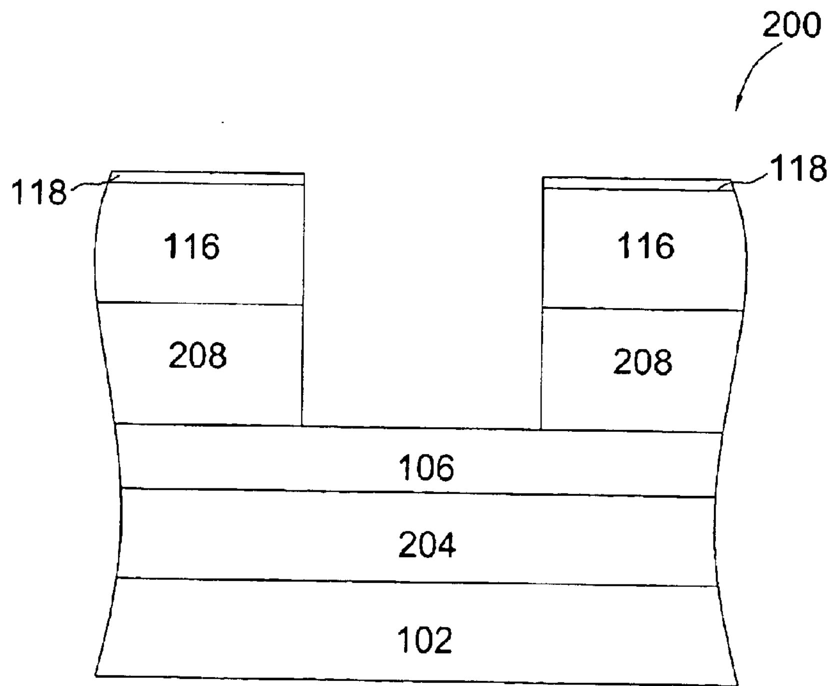


Fig.3B(prior art)

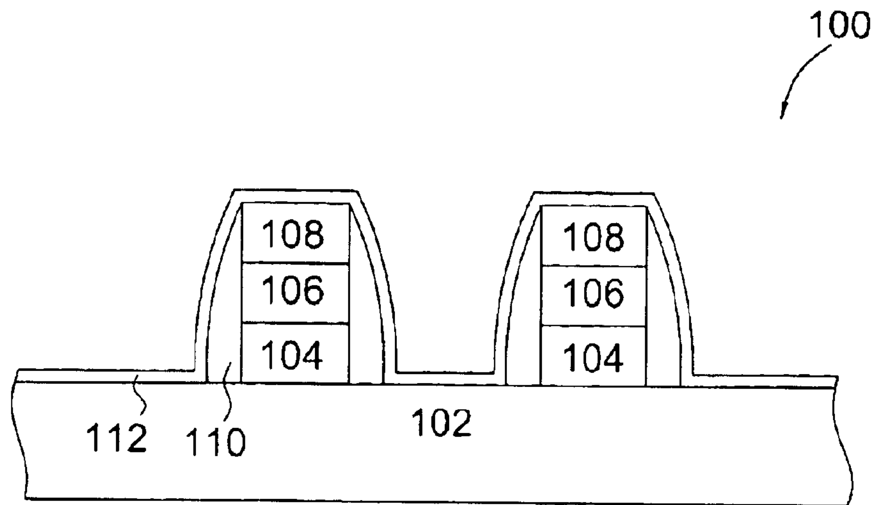


Fig.4A

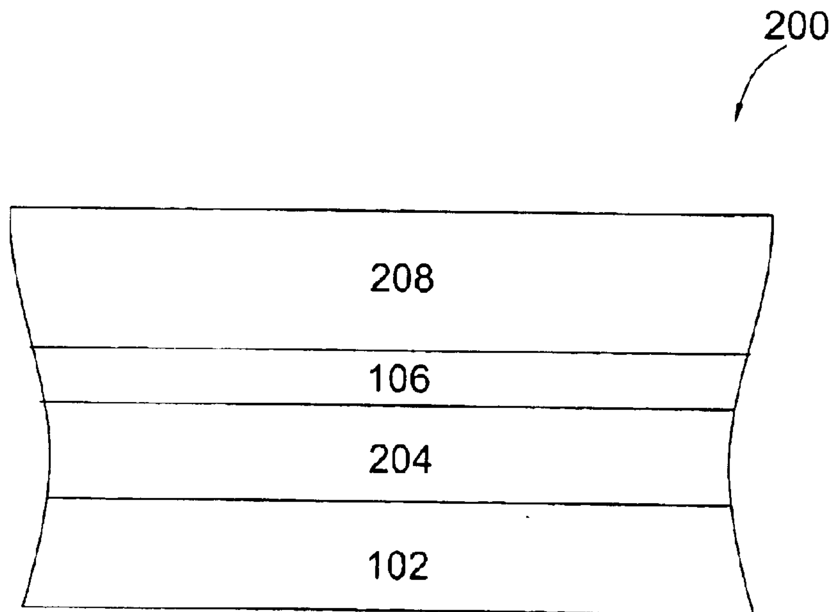


Fig.4B

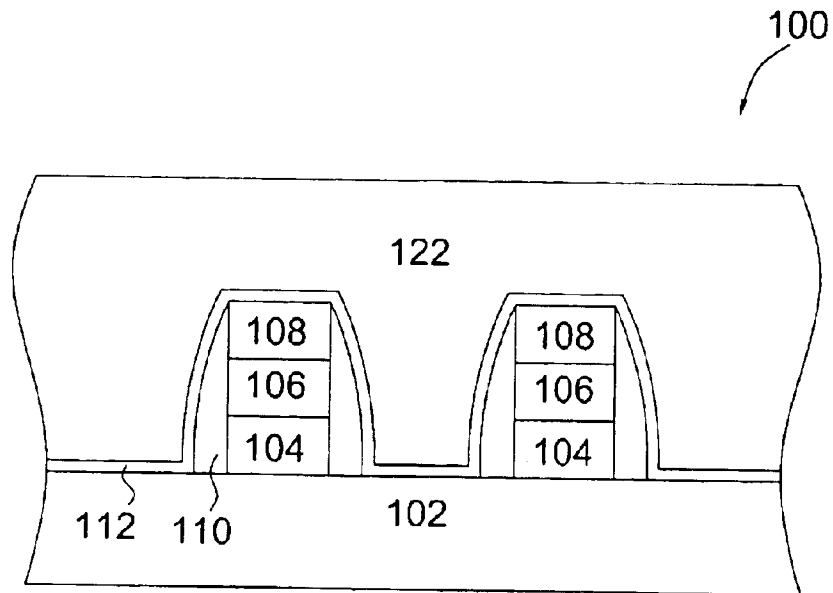


Fig.5A

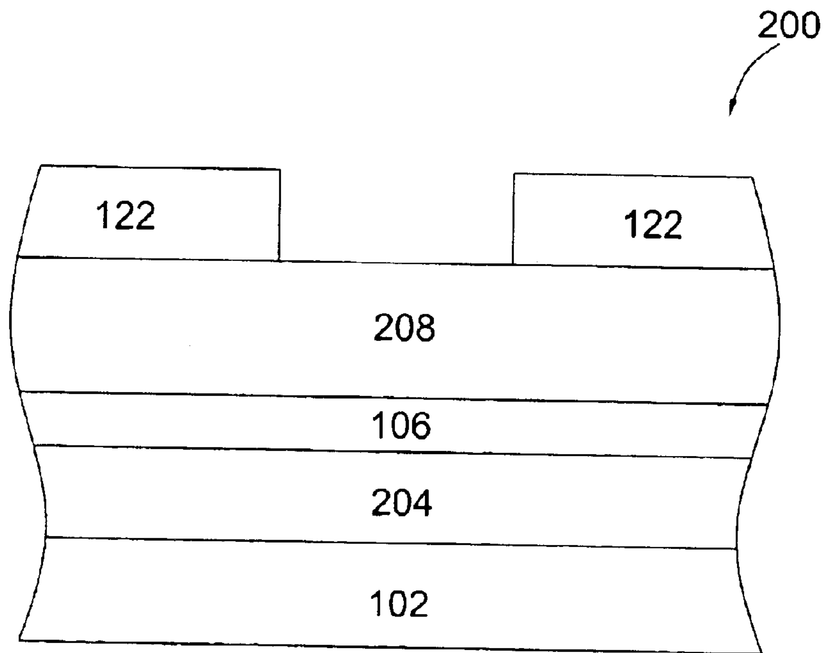


Fig.5B

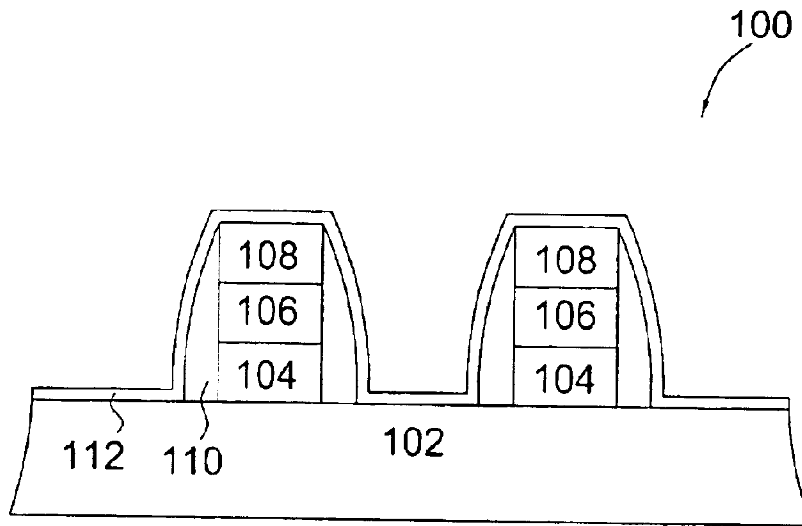


Fig.6A

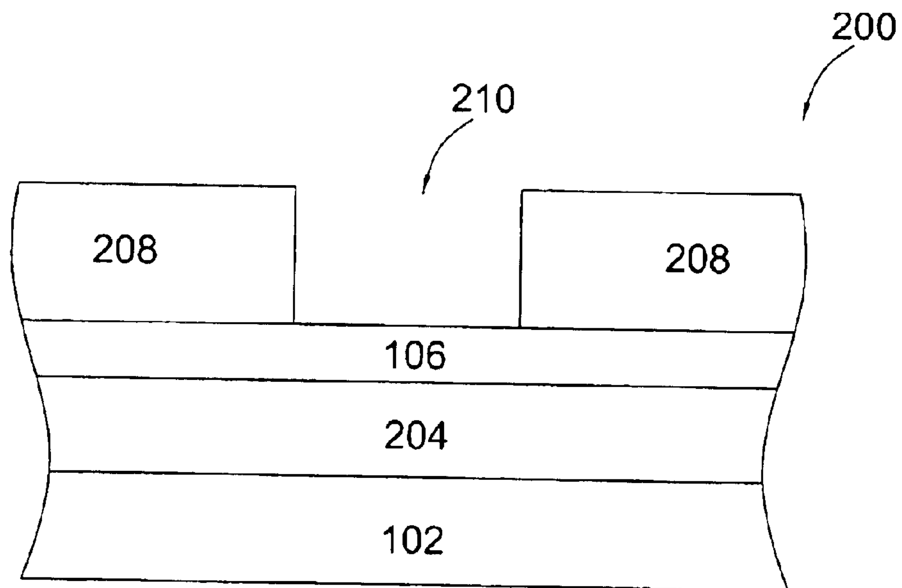


Fig.6B

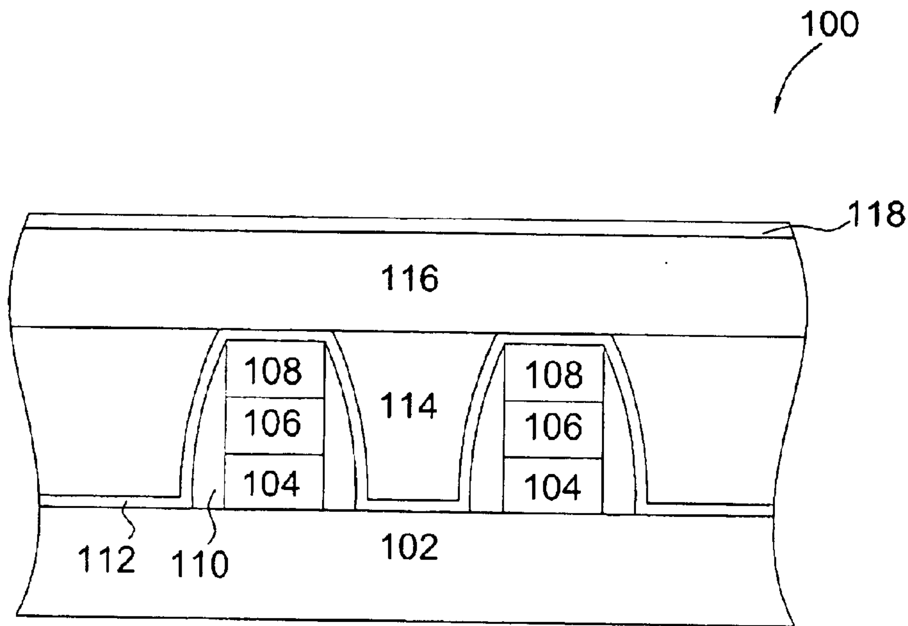


Fig.7A

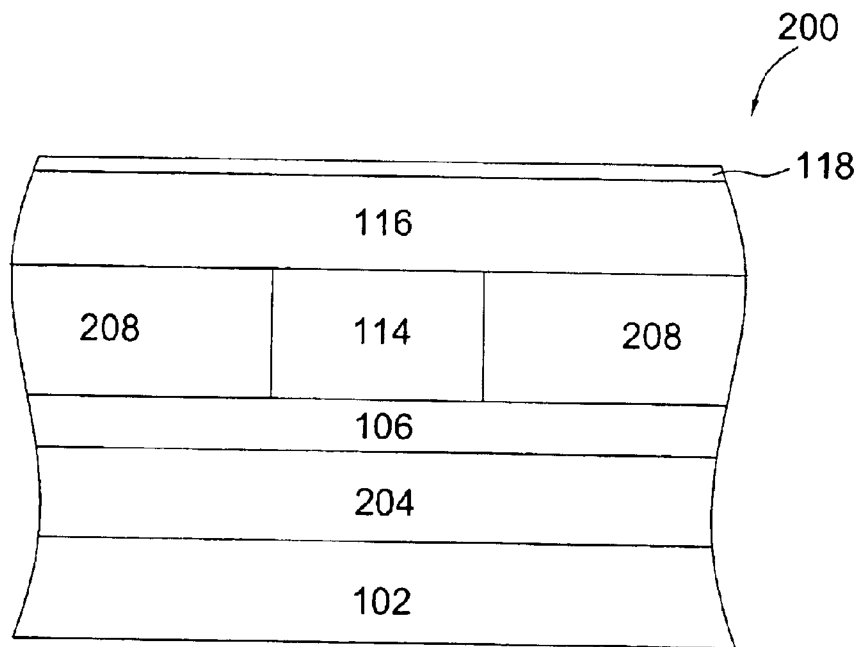


Fig.7B

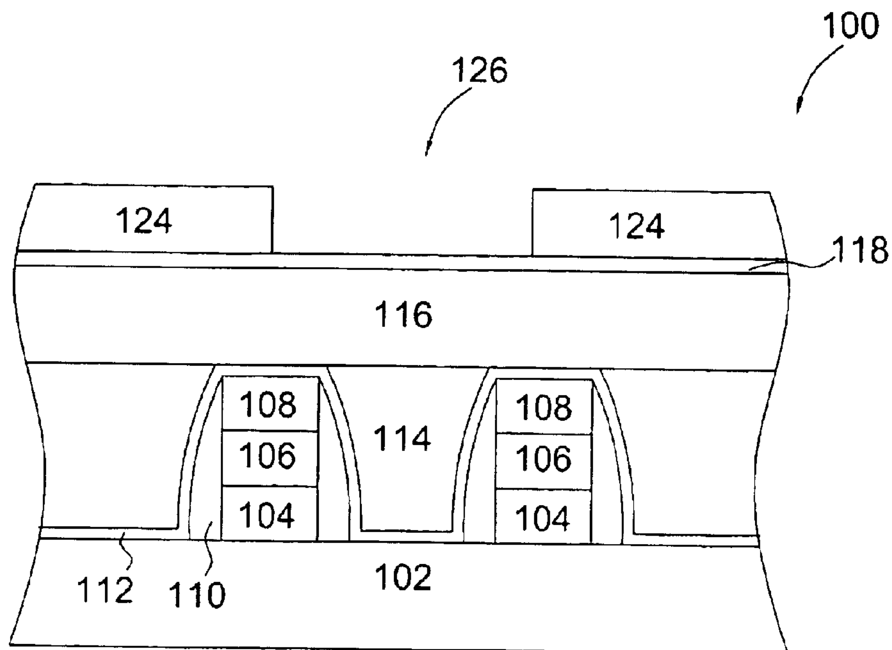


Fig.8A

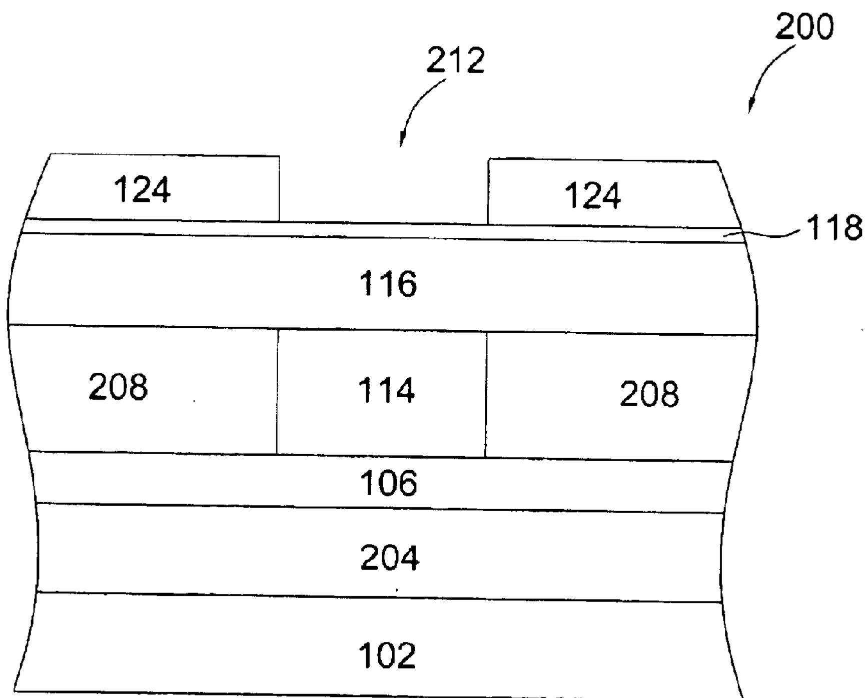


Fig.8B

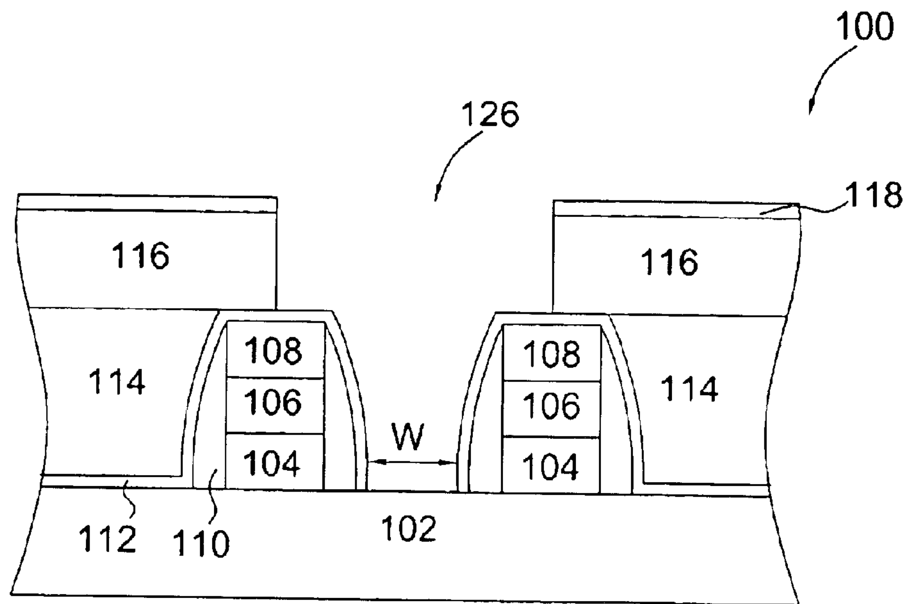


Fig.9A

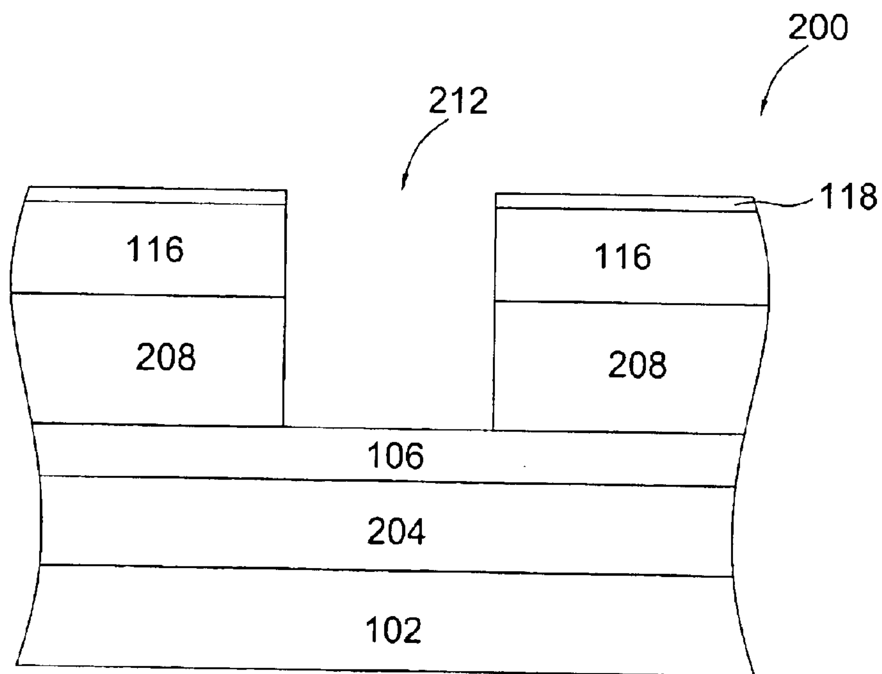


Fig.9B

METHOD FOR FORMING CONTACT

FIELD OF INVENTION

The present invention relates to a method for forming contacts, and particularly, relates to a method for forming memory contacts on a semiconductor device.

BACKGROUND OF THE INVENTION

Most integrated circuits are manufactured by repeating several semiconductor processes, e.g. photolithographing, etching, depositing and doping, and are accomplished with many layers. To transmit signals among those layers, contacts and conductive lines are indispensable to modern semiconductor processes, especially for manufacturing memory chips. The contacts in a memory at least include bit-line contacts and gate contacts, and their manufacturing quality has great effect upon functions of the memory.

FIGS. **1~4** show the steps for forming contacts on a semiconductor device in the prior art. The contacts are positioned on a substrate **102** which has a bit-line contact area **100** and a gate contact area **200**. FIG. **1**A shows the bit-line contact area **100** which includes a first polysilicon layer **104**, a conductive layer **106**, a first dielectric layer **108**, a side wall **110**, a second dielectric layer **112**, a third dielectric layer **114**, a fourth dielectric layer **116** and a second polysilicon layer **118**. FIG. **1**B shows the gate contact area **200** which includes a third polysilicon layer **204**, the conductive layer **106**, a fifth dielectric layer **208**, the fourth dielectric layer **116** and the second polysilicon layer **118**.

Referring to FIG. **1**A and FIG. **1**B, the method of the prior art coats a photoresist **120** on the bit-line contact area **100** as well as the gate contact area **200**, and then etches the two areas. Hence, a bit-line contact is formed on the bit-line contact area **100** as FIG. **2**A shows; however, a gate contact is not formed yet insofar as FIG. **2**B shows. The method of the prior art needs further steps of coating another photoresist **210** on the gate contact area **200**, as FIG. **3**A shows, and then etching the fifth dielectric layer **208** to form the gate contact as FIG. **3**B shows.

This kind of semiconductor process causes the aspect ratio too small to facilitate photoresist removal.

SUMMARY OF THE INVENTION

The present invention provides a method for forming contacts on a semiconductor device, especially for forming memory contacts. The contacts mentioned herein are positioned on a substrate having a bit-line contact area and a gate contact area.

The method of the present invention includes the steps of forming an opening on the gate contact area, depositing a dielectric layer on the bit-line contact area and the opening, coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area, etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening, removing the photoresist, and forming a conductive layer on the bit-line contact opening and the gate contact opening.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A illustrates a sectional view of the bit-line contact area in the prior art;

FIG. **1**B illustrates a sectional view of the gate contact area in the prior art;

FIG. **2**A and FIG. **2**B illustrate sectional views for forming the bit-line contact opening in the prior art;

FIG. **3**A and FIG. **3**B illustrate sectional views for forming the gate contact opening in the prior art;

FIG. **4**A illustrates a sectional view of the bit-line contact area of the present invention;

FIG. **4**B illustrates a sectional view of the gate contact area of the present invention;

FIG. **5**A and FIG. **5**B illustrate sectional views for coating a photoresist to form an opening of the present invention;

FIG. **6**A and FIG. **6**B illustrate sectional views after the photoresist is removed;

FIG. **7**A and FIG. **7**B illustrate sectional views for depositing a dielectric layer;

FIG. **8**A and FIG. **8**B illustrate sectional views for coating another photoresist; and

FIG. **9**A and FIG. **9**B illustrate sectional views for forming the bit-line contact and the gate contact.

DETAILED DESCRIPTION

FIGS. **4~9** show an embodiment of the present invention. FIG. **4**A shows the structure of a bit-line contact area **100** which includes a first polysilicon layer **104**, a conductive layer **106**, a first dielectric layer **108**, a side wall **110** and a second dielectric layer **112**. FIG. **4**B shows the structure of a gate contact area **200** which includes a third polysilicon layer **204**, the conductive layer **106** and a fifth dielectric layer **208**.

The method of the present invention includes the step of forming an opening on the gate contact area **200**. As FIG. **5**A and FIG. **5**B show, the method coats a photoresist **122** on the bit-line contact area **100** and the gate contact area **200** to define an opening pattern on the gate contact area **200** by means of the photolithography technique of the prior art. Next, the method etches the fifth dielectric layer **208** and then removes the photoresist **122**. As FIG. **6**A shows, the structure of the bit-line contact area **100** does not change, but as FIG. **6**B shows, the gate contact area **200** forms an opening **210**.

Then the method deposits a dielectric layer on the bit-line contact area **100** and the opening **210**. As FIG. **7**A and FIG. **7**B show, the dielectric layer includes a third dielectric layer **114** and a fourth dielectric layer **116**. In the embodiment, the third dielectric layer **114** is a borophospho-silicate glass (BPSG) layer. It is noted that an annealing process is preferably executed after the borophospho-silicate glass layer is deposited in order to reduce resistivity. The annealing temperature is 850~950° C. and the deposition depth of the borophospho-silicate glass layer on the bit-line contact area **100** after annealing is 2400~2500 Å. Moreover, the fourth dielectric layer **116** of the embodiment is a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å.

The method of the present invention further includes the step of forming a polysilicon layer **118** as a hard mask when etching the third dielectric layer **114** and the fourth dielectric layer **116**.

Referring to FIG. **8**A and FIG. **8**B, the method of the present invention coats another photoresist **124** to define a bit-line contact opening **126** on the bit-line contact area **100** and a gate contact opening **212** on the gate contact area **200**.

Then the third dielectric layer **114** and the fourth dielectric layer **116** is etched by using the photoresist as a mask to form the bit-line contact opening **126** and the gate contact opening **212**. Next, the method removes the photoresist **124** so that

the bit-line contact opening **126** and the gate contact opening **212** are accomplished as FIG. **9**A and FIG. **9**B show. Finally, a conductive layer is formed on the bit-line contact opening **126** and the gate contact opening **212** to be a medium for signal transmission.

The width W of the bit-line contact opening **126** made by the method of the present invention is 60~70 nm, which is 50~75% wider than that of the prior art. The larger aspect ratio facilitates photoresist removal.

The above description of the preferred embodiments is expected to clearly expound the characteristics of the present invention but not expected to restrict the scope of the present invention. Those skilled in the art will readily observe that numerous modifications and alteration of the apparatus may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the bounds of the claims.

What is claimed is:

1. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a dielectric layer on the bit-line contact area and the opening;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

2. The method of claim **1**, wherein the depositing step further comprises:

depositing a borophospho-silicate glass (BPSG) layer;

annealing the borophospho-silicate glass layer, and

depositing a tetraethyl orthosilicate (TEOS) layer.

3. The method of claim **2**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

4. The method of claim **2**, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

5. The method of claim **2**, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950° C.

6. The method of claim **1**, further comprising forming a polysilicon layer as a hard mask between the depositing step and the coating step.

7. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer;

depositing a tetraethyl orthosilicate (TEOS) layer;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and the tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

8. The method of claim **7**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

9. The method of claim **7**, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

10. The method of claim **7**, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950° C.

11. The method of claim **7**, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.

12. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer under a temperature of 850~950° C.;

depositing a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and tile tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

13. The method of claim **12**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

14. The method of claim **12**, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.

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