US 20190318681A1

(19) **United States**

(12) **Patent Application Publication**

ZHANG et al.

(10) **Pub. No.: US 2019/0318681 A1**

(43) **Pub. Date: Oct. 17, 2019**

(54) **INTEGRATED CIRCUIT, MOBILE PHONE AND DISPLAY**

(71) Applicants: **Kunshan New Flat Panel Display Technology Center Co., Ltd.**, Kunshan, Jiangsu (CN); **KunShan Go-Visionox Opto-Electronics Co., Ltd**, Kunshan, Jiangsu (CN)

(72) Inventors: **Tingting ZHANG**, Kunshan, Jiangsu (CN); **Yanqian SONG**, Kunshan, Jiangsu (CN); **Siming HU**, Kunshan, Jiangsu (CN); **Hui ZHU**, Kunshan, Jiangsu (CN); **Li LIN**, Kunshan, Jiangsu (CN)

(21) Appl. No.: **16/322,071**

(22) PCT Filed: **Jan. 5, 2018**

(86) PCT No.: **PCT/CN2018/071494**

§ 371 (c)(1),
(2) Date: **Jan. 30, 2019**

(30) **Foreign Application Priority Data**

Jan. 6, 2017 (CN) 201710009707.2

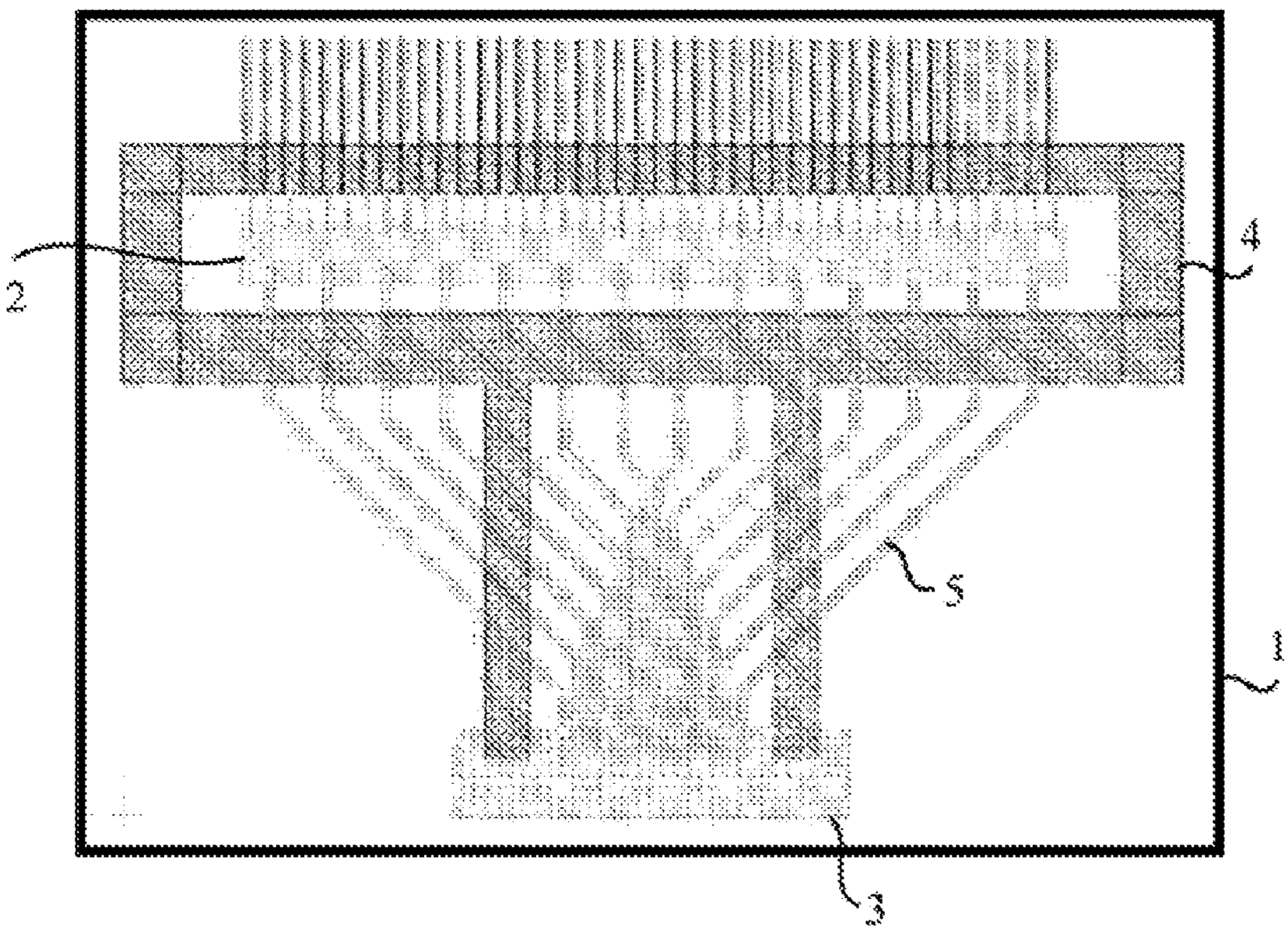
Publication Classification

(51) **Int. Cl.**
G09G 3/20 (2006.01)

(52) **U.S. Cl.**
CPC ... ***G09G 3/2092*** (2013.01); *G09G 2300/0426* (2013.01); *G09G 2310/0297* (2013.01); *H04M 1/0202* (2013.01); *G09G 2320/0223* (2013.01); *G09G 2330/02* (2013.01); *G09G 2310/0272* (2013.01)

(57) **ABSTRACT**

An integrated circuit, a mobile phone and a display are provided with the integrated circuit. The integrated circuit includes a substrate, a data distributor and a data driver distributed on the substrate. A power line trace gap is provided within the data distributor; a first data line connected to the data driver and to the data distributor; and a first power line connected to the data driver and passing through the power line trace gap.



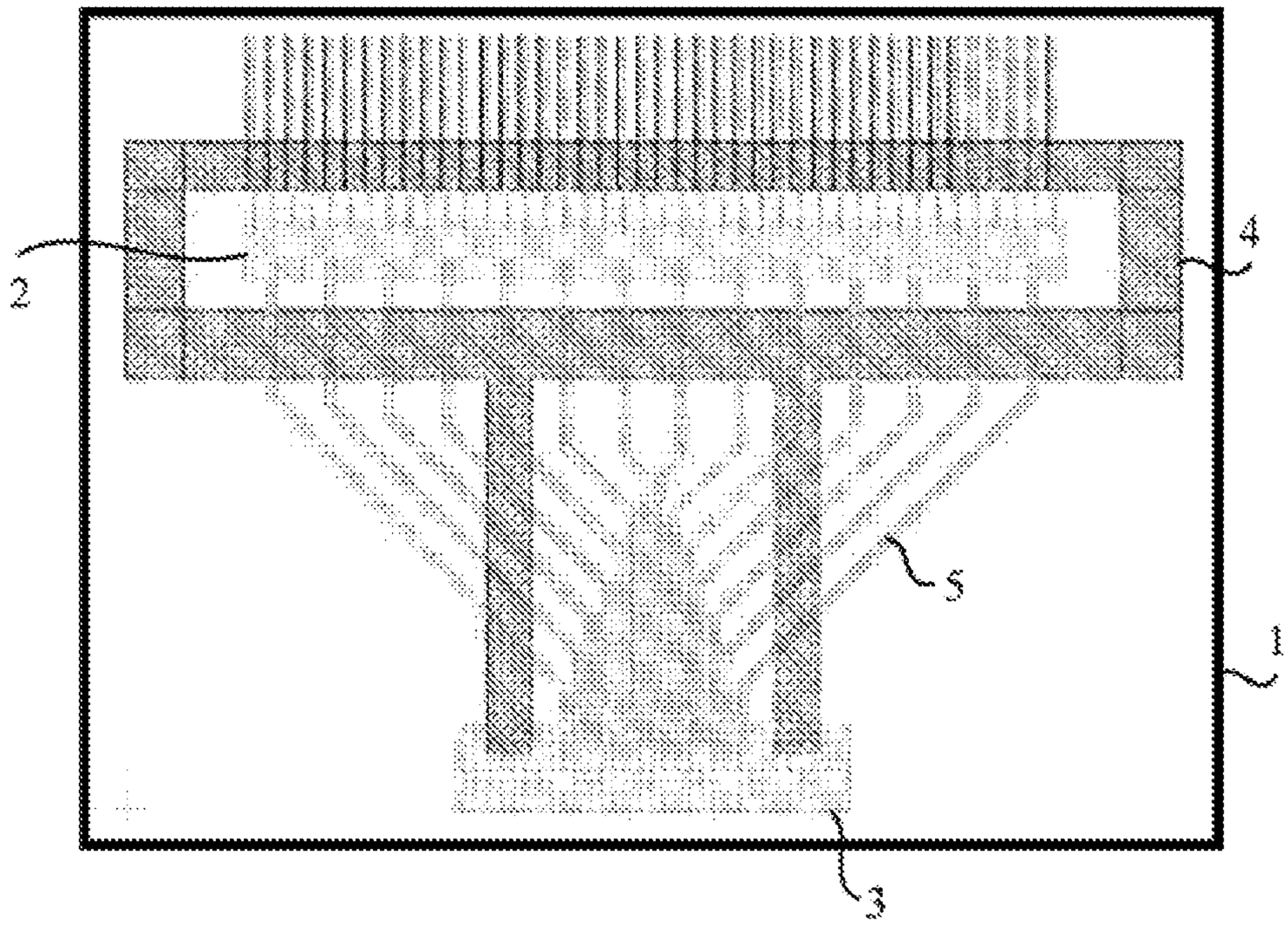


FIG.1

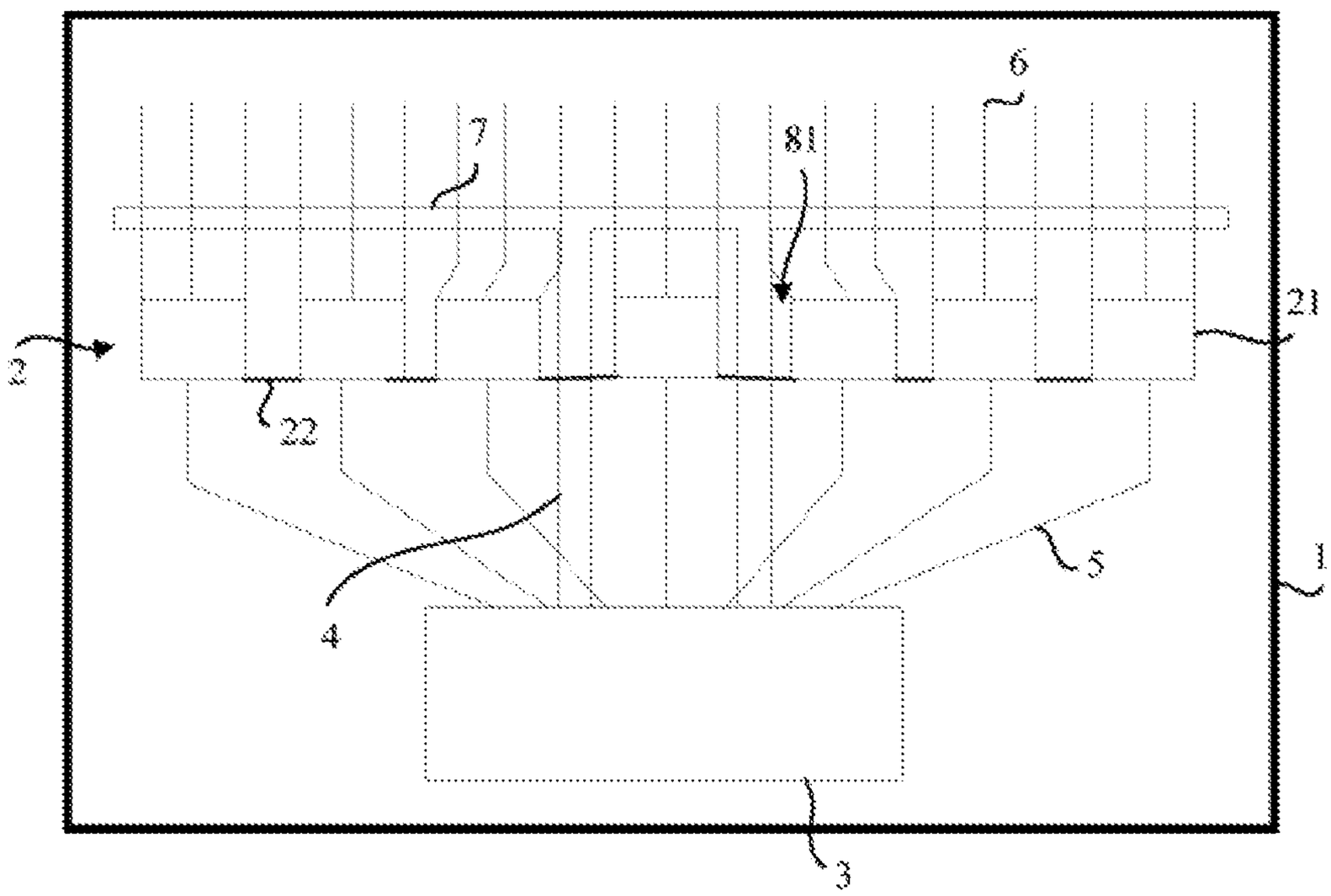


FIG.2

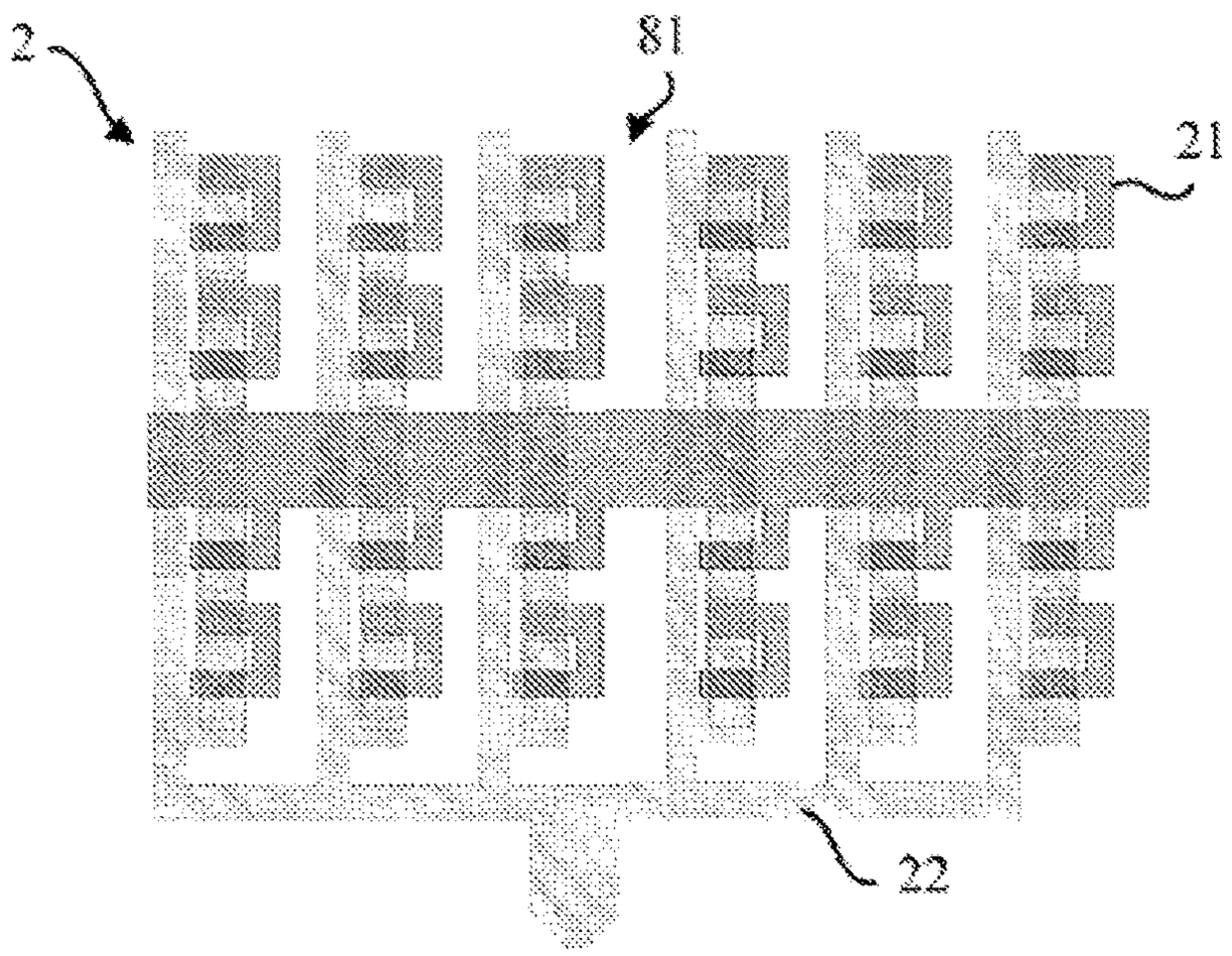


FIG.3

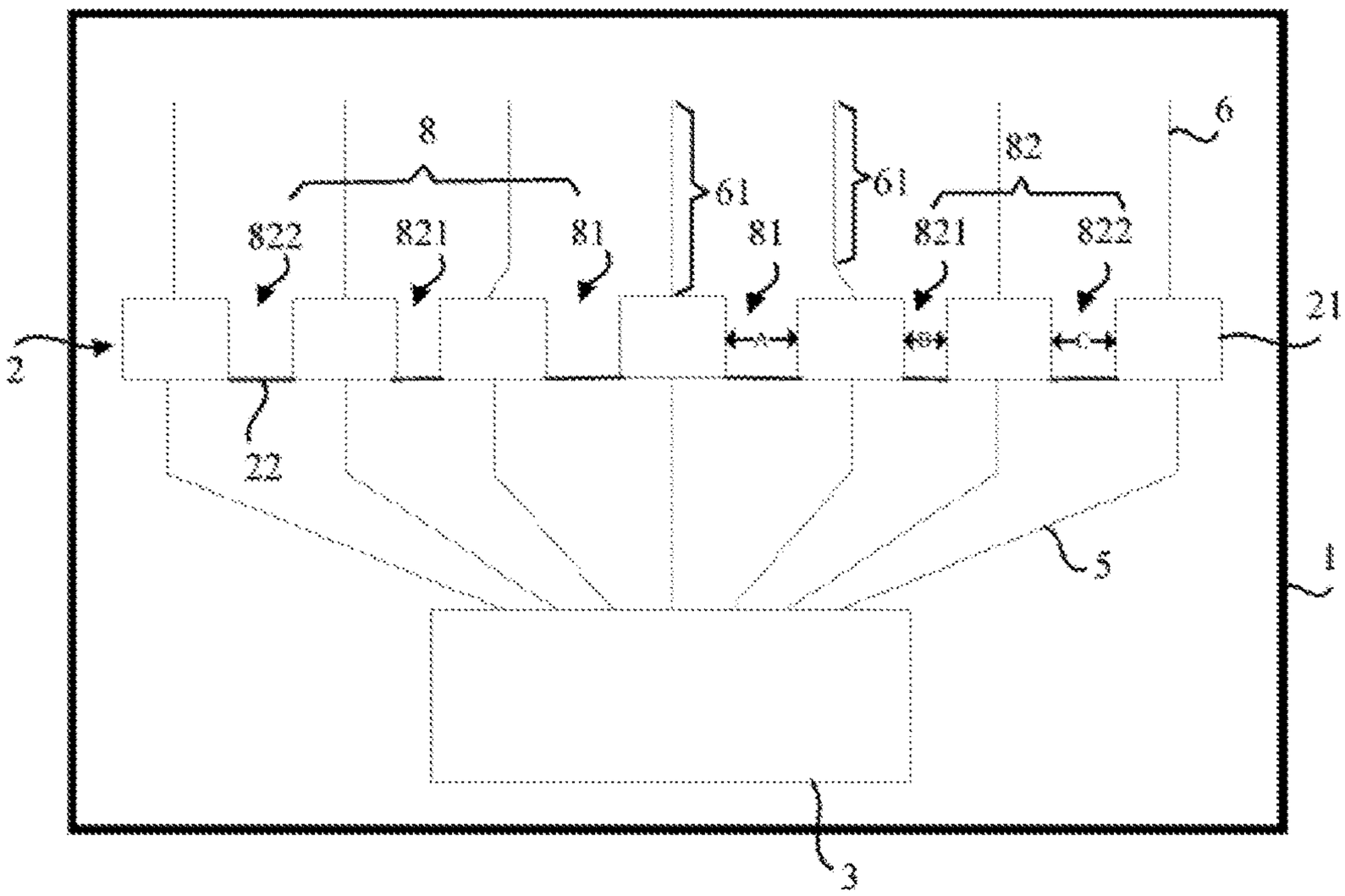


FIG.4

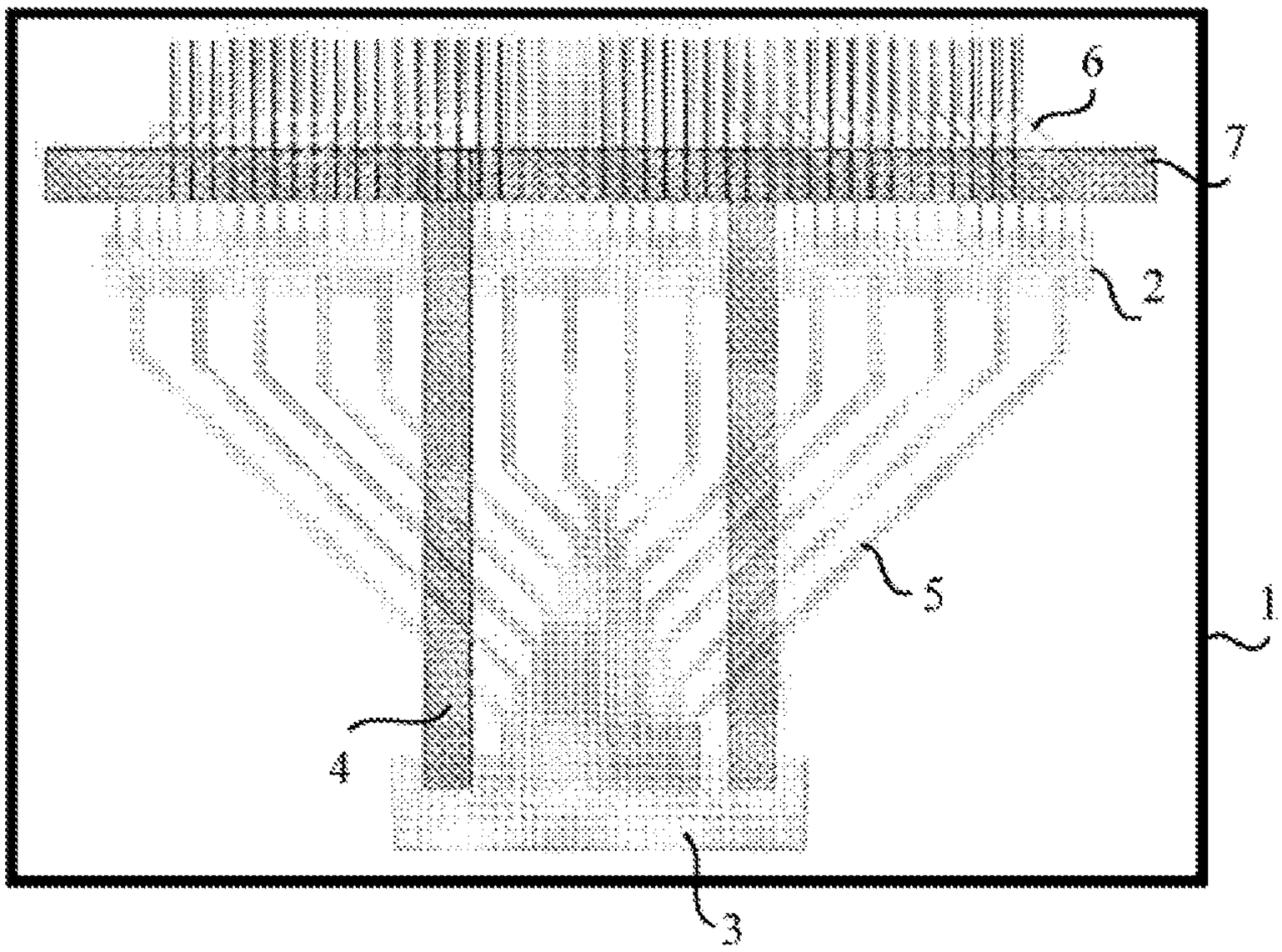


FIG.5

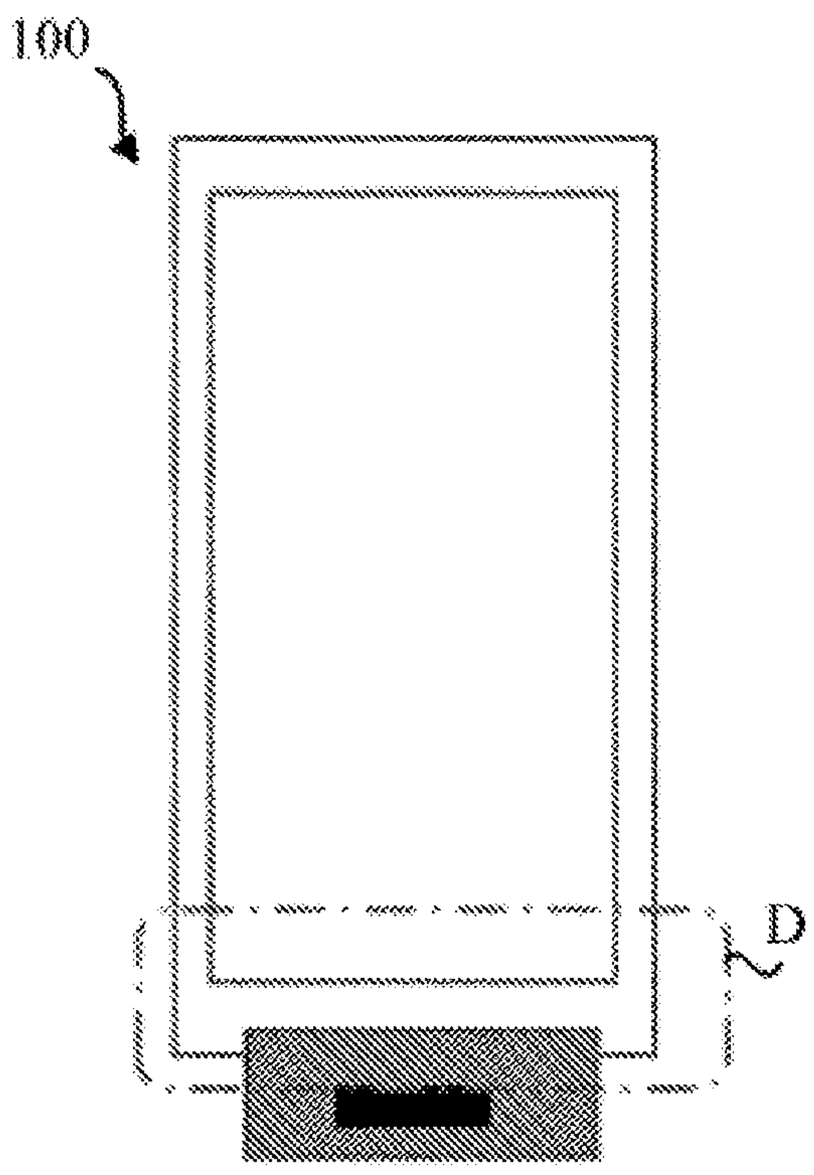


FIG.6

INTEGRATED CIRCUIT, MOBILE PHONE AND DISPLAY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 201710009707.2, filed on Jan. 6, 2017 and titled "INTEGRATED CIRCUIT, MOBILE PHONE AND DISPLAY", the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

[0002] This application relates to circuit technical field, particularly to an integrated circuit, a mobile phone and a display provided with the integrated circuit.

BACKGROUND

[0003] An integrated circuit, also known as a microcircuit, microchip or chip, is a microelectronic device or component. An integrated circuit is a micro-structure having required circuit functions, formed by using a certain process to interconnect the elements and circuits required in a circuit on one or several substrates.

[0004] The integrated circuit can be applied to devices in the field of military, communication, remote control, and the like. Taking an integrated circuit applied to a mobile phone as an example, as shown in FIG. **1**, a data distributor **2** (DEMUX, also referred to as a demultiplexer), a data driver **3**, and a power line **4** and a data line **5** connected to the data driver **3** are integrated on the substrate **1**. Here, the data line **5** is used to transmit data signals. The data distributor **2** is used to distribute the signals transmitted by the data line **5** into multipath signals, so that it is possible to ensure fewer data lines connected to the data driver **3**. The power line **4** is used to transfer power to supply power to the data driver **3**.

[0005] Generally, after the power line **4** is drawn out of the data driver **3**, it is necessary to make the power line bypass the data distributor **2**, so as to extend to other areas of the substrate **1** to supply power to devices in other areas. However, this causes the parasitic capacitance across the data line **5** to be large, so that the transmission of the data signal can be blocked, which results in delay of the data signal.

SUMMARY

[0006] The embodiments of the present application provide an integrated circuit to solve the technical problem in the prior art that the parasitic capacitance on the data line is so large such that the data signal may be delayed.

[0007] The embodiments of the present application also provide a mobile phone and a display to solve the technical problem in the prior art that the parasitic capacitance on the data line is so large such that the data signal can be delayed.

[0008] The following technical solution can be adopted by the embodiments of the present application.

[0009] An integrated circuit of the present application comprises a substrate, a data distributor and a data driver distributed on the substrate, wherein the data distributor having a power line trace gap provided therein; a first data line connected to the data driver and the data distributor; and a first power line connected to the data driver and passing through the power line trace gap.

[0010] Optionally, the data distributor comprises a plurality of functional units distributed on the substrate and connected to the first data line, wherein two adjacent functional units are connected to each other by wires embedded on the substrate, and the power line trace gap is provided between two adjacent functional units.

[0011] Optionally, the two adjacent functional units has a gap defined therebetween, wherein the gap comprises the power line trace gap and a vacant gap which is not provided with the first power line, wherein a width of the power line trace gap is larger than that of the vacant gap.

[0012] Optionally, a width of a first vacant gap adjacent to the power line trace gap is less than a width of a second vacant gap spaced apart from the power line trace gap by at least one of the first gap; or the width of respective vacant gap is the same.

[0013] Optionally, a sum of a width of a single power line trace gap and a width of a single first vacant gap is twice of a width of a single second vacant gap, when the width of the first vacant gap is less than the width of the second vacant gap.

[0014] Optionally, the first power line is configured to linearly extend and pass through the data distributor after being drawn from the data driver.

[0015] Optionally, at least two first power lines are provided, and are configured to be integrated into one second power line after passing through the data distributor.

[0016] Optionally, the integrated circuit further comprises a plurality of second data lines connected to the data distributor and intersected with scan lines of the integrated circuit, wherein the second data line each comprises a second data line portion linearly extending, the gaps between two adjacent second data line portions are the same.

[0017] A mobile phone of the present application comprises a housing and an integrated circuit provided within the housing, wherein the integrated circuit is any one of the integrated circuit mentioned above.

[0018] A display of the present application comprises a housing and an integrated circuit provided within the housing, wherein the integrated circuit is any one of the integrated circuit mentioned above.

[0019] The following advantageous effects can be achieved by at least one of the technical solutions adopted by the embodiments of the present application:

[0020] In the technical solution adopted by the embodiment of the present application, a data distributor, a data driver, a first data line and a first power line are embedded on the substrate, wherein the first power line passes through a power line trace gap within the data distributor. In this way, the length of the intersection of the first data line and the first power line can be decreased. Since the intersection area of the first data line and the first power line has a parasitic capacitance, when the intersection area of the first data line and the first power line decreases, the parasitic capacitance accumulated to the first data line can be correspondingly reduced, therefore the hindrance of the parasitic capacitance of the first data line to the data signal can be reduced, thereby the delay of the data signal can be reduced. Thus, the present application proposes a technical solution that the parasitic capacitance of the data lines can be reduced, thereby reducing the delay of the data signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Accompanying drawings illustrated here are used for providing further understanding of the present application. The drawings form a part of the application. Exemplary embodiments of the present application and the description thereof are intended to interpret the present application rather than improperly limit the present application. In the drawings:

[0022] FIG. **1** is a structural schematic view of an integrated circuit in the prior art;

[0023] FIG. **2** is a structural schematic view of the first kind of integrated circuit provided by the embodiments of the present application;

[0024] FIG. **3** is a structural schematic view of the data distributor provided by the embodiments of the present application;

[0025] FIG. **4** is a structural schematic view of the integrated circuit provided by the embodiments of the present application with the power line removed;

[0026] FIG. **5** is a structural schematic view of the second kind of integrated circuit provided by the embodiments of the present application;

[0027] FIG. **6** is a structural schematic view of a mobile phone which is provided with an integrated circuit, provided by the embodiments of the present application.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0028] In order to make the purpose, the technical solution and advantages of the present application more clear, the technical solution of the present application will be described clearly and completely in the following with reference to the specific embodiments and the corresponding drawings. Obviously, the described embodiments are merely a part of the embodiments of the present application rather than all of the embodiments. Based on the embodiments in the present application, all the other embodiments obtained by a person skilled in the art without creative work will fall into the protection scope of the present application.

[0029] Refer to FIG. **2**, the integrated circuit of the present application includes a substrate **1**, a data distributor **2**, a data driver **3**, a first power line **4**, a plurality of first data lines **5**, and a plurality of second data lines **6** respectively distributed on the substrate **1**. The substrate **1** have multiple layers, the first data lines **5** and the second data lines **6** may be located on the same layer, the first data lines **5** and the first power line **4** are located on different layers, the layer on which the data lines **5** is located and the layer on which the first power line **4** is located may be spaced by an insulating layer, the data distributor **2** and the data driver **3** are respectively passing through the layer on which the data lines **5** is located and the layer on which the first power line **4** is located.

[0030] Each of the first data lines **5** is connected to the data driver **3**, and the data driver **3** is configured to drive the first data line **5**, transmit the data signal to the first data line **5**, and transmit the data signal through the first data line **5**. The data distributor **2** is connected to the first data line **5** and the second data line **6** for shunting the data signal transmitted by the first data line **5** and transmitting the shunted data signal to the second data line **6**. The second data line **6** is disposed across the scan line (not shown) of the integrated circuit.

[0031] As can be seen in FIGS. **2** and **3**, a power line trace gap **81** is provided in the data distributor **2**. The first power line **4** passes through the power line trace gap **81** after being drawn from the data driver **3**. The first power line **4** may be provided with at least two power lines, and each of the first power lines **4** is located in a different power line trace gaps **81**, that is, one of the first power line **4** is disposed in one power line trace gap **81**. Each of the first power lines **4** can be integrated into a second power line **7** after passing through the data distributor **2**, so that the extension direction of the second power line **7** can be substantially parallel to the extension direction of the data driver **3**, so as to facilitate the arrangement of other power lines connected to the second power line **7** (other power lines except the first power line **4**).

[0032] The first power line **4** passes through the power line trace gap **81** without bypassing the data distributor **2**. This has little effect on a design of the first power line **4**, and has little effect on the resistance voltage drop of the first power line **4**; the length of a intersection of the first data line **5** and the first power line **4** can be reduced. Thereby, the parasitic capacitance of the first data line **5** can be reduced, in turn, the delay of the data signal can be reduced.

[0033] In a specific embodiment, as can be seen in FIG. **4**, the data distributor **2** includes a plurality of functional units **21** distributed on the substrate **1**, and two adjacent functional units **21** are connected by wires **22** embedded in the substrate **1**. The plurality of functional units **21** are disposed in a row, and its orientation is substantially parallel to the extension direction of the data driver **3**. Each functional unit **21** is connected to a part of first data lines **5** and a part of second data lines **6**. The function of each functional unit **21** can be specifically set according to requirements.

[0034] A certain gap **8** is left between two adjacent functional units **21**. The gap **8** includes a power line trace gap **81**, that is, a power line trace gap **81** is disposed between two adjacent functional units **21** to facilitate disposing the power line trace gap **81**. The first power line **4** can linearly extend and pass through the data distributor **2** after being drawn from the data driver **3** in the process of arranging the power line trace gap **81**, therefore the length of the first power line **4** can be further decreased and the length of the intersection of the first power line **5** and the first data line **4** can be decreased.

[0035] Under normal conditions, the number of the first power lines **4** drawn from the data driver **3** is generally not more than three, and the number of the functional units **21** is more than ten. Therefore, the gap **8** between the functional units **21** may include, in addition to the power line trace gap **81**, a vacant gap **82** which is not used to receive the first power line **4**. The width of the vacant gap **82** may be smaller than the width of the power line trace gap **81** to reduce the length of the data distributor **2**, so that the data distributor **2** can be distributed over the substrate **1**.

[0036] In one example, the power line has a diameter of approximately 100 μm (micrometers), the power line trace gap **81** may have a width of 110 μm, and the vacant gap **82** may have a width of less than 100 μm. Of course, the example is merely an illustrative description. In practice, it can be set according to specific requirements.

[0037] Further, the width B of the first vacant gap **821** may be smaller than the width C of the second vacant gap **822**. The first vacant gap **821** is a vacant gap **82** adjacent to the power line trace gap **81**, and the second vacant gap **822** is a vacant gap **82** spaced apart from the power line trace gap **81** by at least one the first gaps. In the comparison of the routing manner of the first data line **5** and the routing manner of the

second data line **6** under the situation that the width of the first vacant gap and the width of the second vacant gap are equal, the second data line **6** connected to the first functional unit (the functional unit **21** between the power line trace gap **81** and the first vacant gap **821**) has a greater bending degree, the second data line **6** connected to the second functional unit (other functional units **21** except the first functional unit) has a smaller bending degree or even extend linearly. The width B of the first vacant gap **821** is smaller than the width C of the second vacant gap **822**, which is particularly suitable for the scenario where the resolution of the pixels of the integrated circuit is low and the number of the functional units **21** is fewer.

[0038] Further, a sum of a width A of a single power line trace gap **81** and a width B of a single first vacant gap **821** is approximately twice that of a width C of a single second vacant gap **822**. Refer to the above example, the width of the first vacant gap **821** may be 50 μm, and the width of the second vacant gap **822** may be 80 μm. Thus, the second data line **6** connected to the first functional unit needs to be bent by a section, and then extends linearly, and the other second data lines **6** can be linearly extended, thus the wiring difficulty can be reduced and the wiring efficiency can be improved.

[0039] As shown in FIG. **4**, after the second data line **6** is set, the second data line **6** may include a second data line portion **61** linearly extended. The gaps between two adjacent second data line portions **61** may be equal, thereby effectively supplying gray scale signal voltage to respective pixel electrode of the integrated circuit.

[0040] Of course, the widths of respective vacant gap of the data distributor **2** may be substantially the same (the width of the first vacant gap is substantially the same as the width of the second vacant gap). In this case, as shown in FIG. **5**, the second data line **6** can be bent as needed. Other structures in FIG. **5** (including the substrate **1**, the data driver **3**, the first power line **4**, the first data line **5**, the second power line **7**, etc.) may be substantially the same as the other structures shown in FIGS. **2** to **4** which will not be described in detail here. The widths of the vacant gaps are the same, and are particularly suitable for the scenario where the resolution of the pixels of the integrated circuit is high and the number of functional units is large.

[0041] Of course, the first vacant gap **821** and the second vacant gap **822** can also be provided in other manners, which will not be described in detail herein.

[0042] In addition, it should be noted that, as can be seen from Table 1, when the voltage of the first power line **4** changes, the parasitic capacitance of the first data line **5** also changes.

TABLE 1

data	Prior art			the present application		
delav	R (Ω)	C (f)	RC	R (Ω)	C (f)	RC
T1	4.38E+03	2.46E−11	1.08E−07	693	1.52E−12	1.05134E−09
T2	1.00E+03	2.00E−14	2.00E−11	1.00E+03	2.00E−14	2E−11
T3	3.99E+03	8.52E−12	3.40E−08	4201.68	7.91E−12	3.32512E−08

[0043] In Table 1, T1, T2 and T3 represent the voltage of the first power line **4**, the voltage of T1 is greater than the voltage of T3, the voltage of T3 is greater than the voltage of T2, and the voltage of T2 is substantially zero;

[0044] R represents the resistance of the first data line **5**;

[0045] C represents the parasitic capacitance of the first data line **5**;

[0046] RC represents the resistance-capacitance of the first data line **5**.

[0047] It can be seen from Table 1 that with the technical solution of the present application, the parasitic capacitance of the first data line **5** can be effectively reduced; as can also be seen from Table 1, due to adoption of the technical solution of the present application, the larger the voltage of the first power line **4**, the more the parasitic capacitance of the first data line **5** can be reduced (relative to that of the prior art).

[0048] The present application also provides a mobile phone **100** with a housing and an integrated circuit (as shown in FIG. **6**, wherein enlargement of an area D is a schematic structural view as shown in FIG. **5**) and a display with a housing and an integrated circuit. The integrated circuit of the mobile phone **100** and the display are disposed in the housing, and the integrated circuit is the integrated circuit mentioned above.

[0049] In the mobile phone and the display, the first power line passes through the power line trace gap inside the data distributor. Thus, the length of the intersection of the first data line and the first power line can be decreased. Since a parasitic capacitance is provided in the intersection area of the first data line and the first power line, when the intersection area of the first data line and the first power line decreases, the parasitic capacitance accumulated to the first data line can be correspondingly reduced, therefore the hindrance of the parasitic capacitance of the first data line to the data signal can be reduced, thereby the delay of the data signal can be reduced.

[0050] The above is merely the embodiments of the present application and is not intended to limit the present application. Various changes and modifications can be made to the present application by a person skilled in the art. Any modifications, equivalents, improvements, etc. made within the spirits and principles of the present application are intended to be included within the scope of the appended claims.

1. An integrated circuit, comprising:

a substrate,

a data distributor and a data driver distributed on the substrate, the data distributor having a power line trace gap provided therein;

a plurality of first data lines connected to the data driver and the data distributor; and

at least one of first power lines connected to the data driver and passing through the power line trace gap.

2. The integrated circuit according to claim **1**, wherein the data distributor comprises a plurality of functional sub-distributors distributed on the substrate and connected to the first data lines, the substrate has a plurality of wires distrib-

uted thereon, wherein two adjacent functional sub-distributors are connected to each other by the plurality of wires, and the power line trace gap is provided between two adjacent functional sub-distributors.

3. The integrated circuit according to claim **2**, wherein the two adjacent functional sub-distributors has a gap defined therebetween, the gap comprises the power line trace gap and a vacant gap not provided with the first power line, and a width of the power line trace gap is larger than that of the vacant gap.

4. The integrated circuit according to claim **3**, wherein a width of a first vacant gap adjacent to the power line trace gap is less than a width of a second vacant gap spaced apart from the power line trace gap by at least one of the first gaps.

5. The integrated circuit according to claim **4**, wherein a sum of a width of a single power line trace gap and a width of a single first vacant gap is twice of a width of a single second vacant gap, when the width of the first vacant gap is less than the width of the second vacant gap.

6. The integrated circuit according to claim **3**, wherein the width of respective vacant gap is the same.

7. The integrated circuit according to claim **1**, wherein the first power line is configured to linearly extend and pass through the data distributor after being drawn from the data driver.

8. The integrated circuit according to claim **1**, wherein the at least one of first power lines comprise at least two of the first power lines, and are integrated into one second power line after passing through the data distributor.

9. The integrated circuit according to claim **1**, further comprising a plurality of second data lines connected to the data distributor and intersected with scan lines of the integrated circuit, wherein each of the second data lines comprises a second data line portion that linearly extends, the gaps between two adjacent second data line portions are the same.

10. A mobile phone, comprising a housing and an integrated circuit provided within the housing, wherein the integrated circuit is the integrated circuit according to claim **1**.

11. A display, comprising a housing and an integrated circuit provided within the housing, wherein the integrated circuit is the integrated circuit according to claim **1**.

* * * * *