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(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME**

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USPC **257/684**; 438/121; 438/106

(57) **ABSTRACT**

A semiconductor device includes a semiconductor substrate provided with a predetermined element and having wirings formed on its main surface connected to back wirings by a plurality of through silicon vias (TSVs), and a conductive cover which covers the main surface of the semiconductor substrate. The semiconductor substrate and the conductive cover are bonded to each other with a conductive bonding member. The TSV bonded to the conductive cover with the conductive bonding member is connected to an external electrode pad to which a ground potential is supplied.

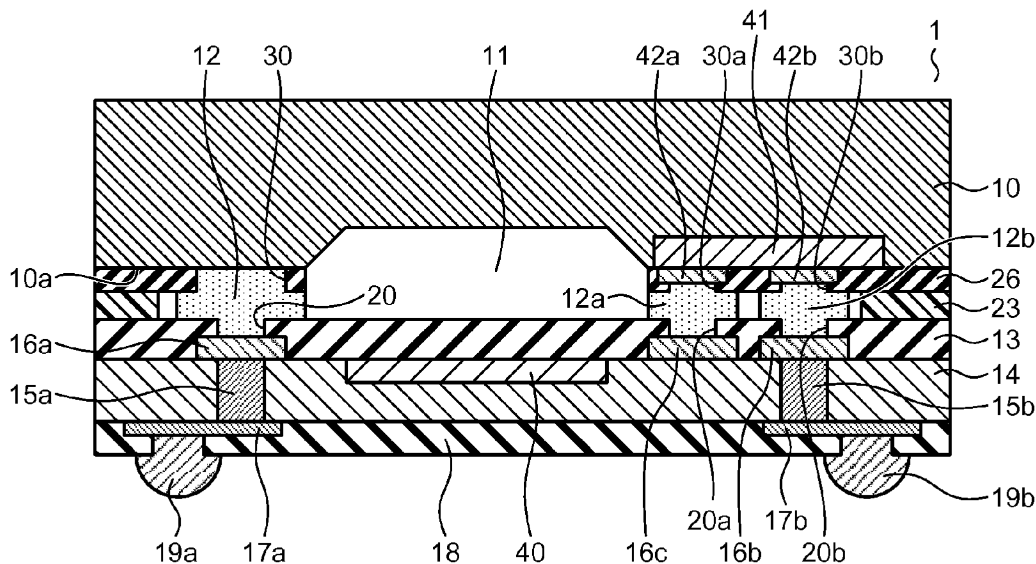


FIG.1

FIG.2A

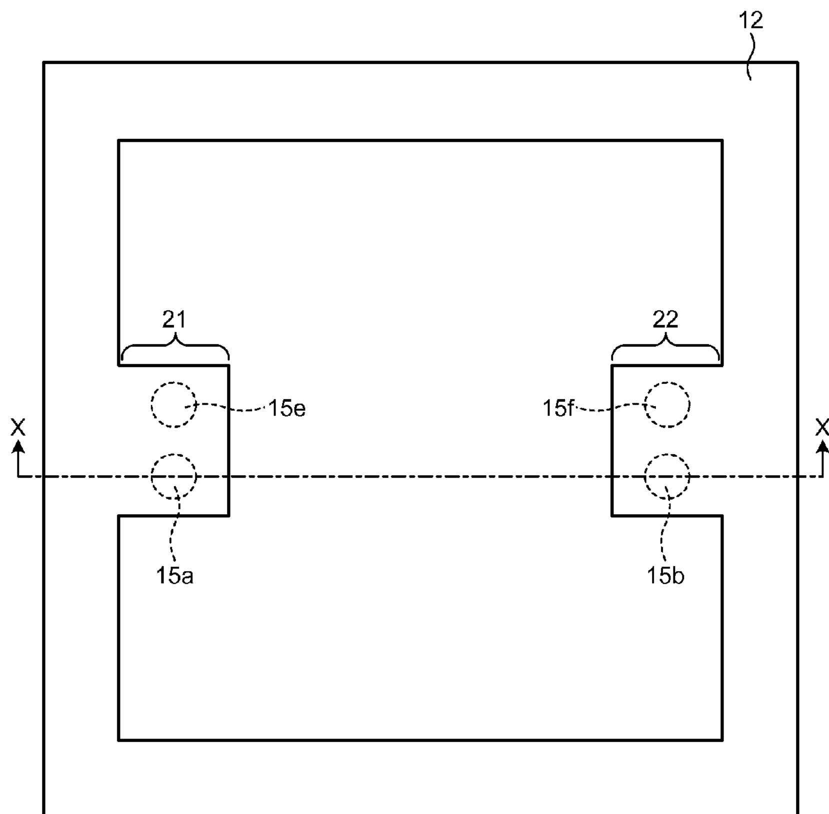


FIG.2B

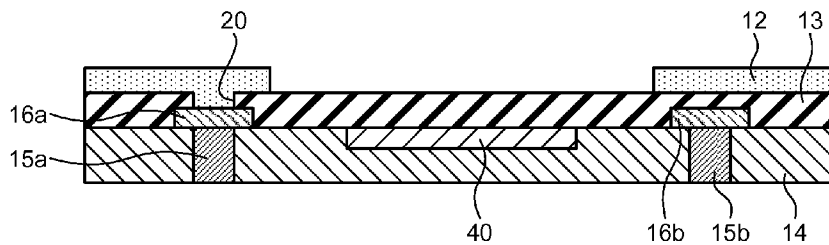


FIG.3A

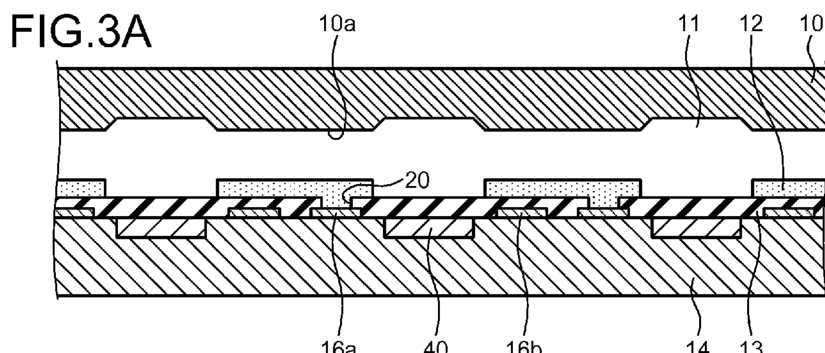


FIG.3B

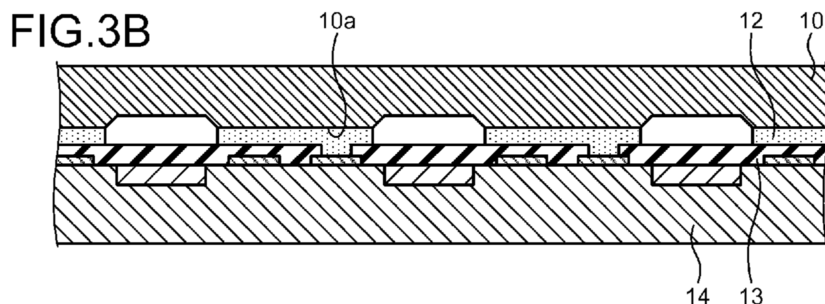


FIG.3C

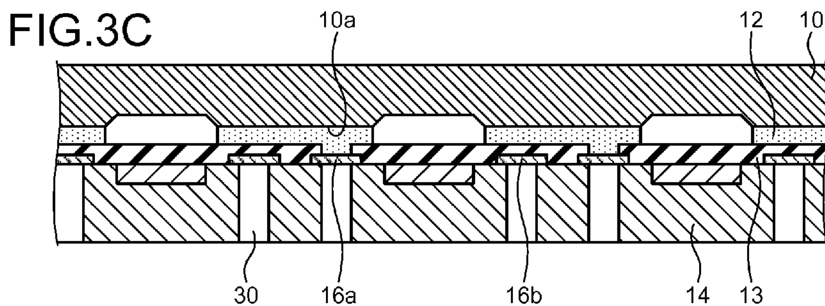


FIG.3D

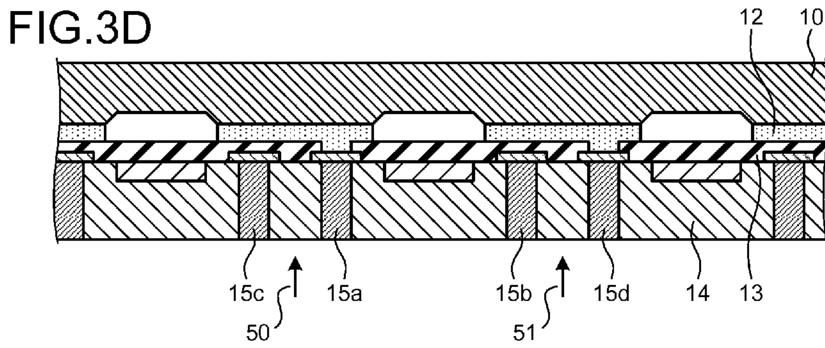


FIG.4A

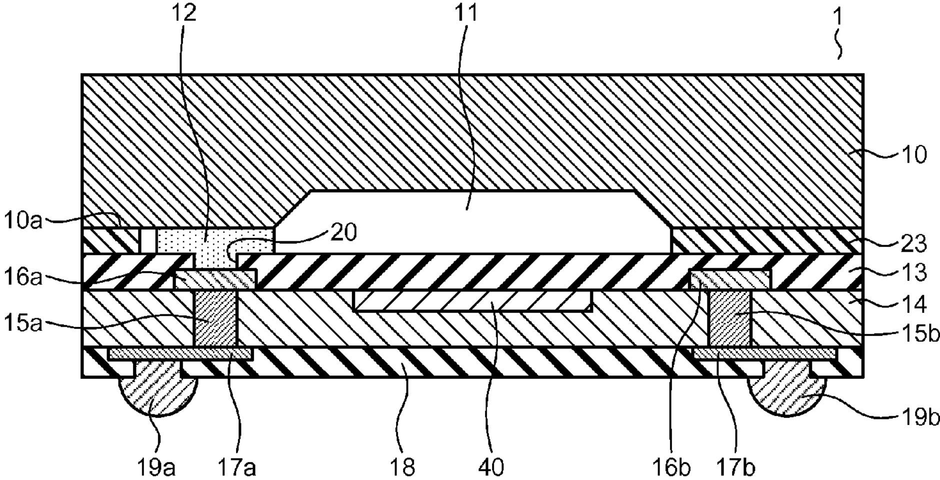


FIG.4B

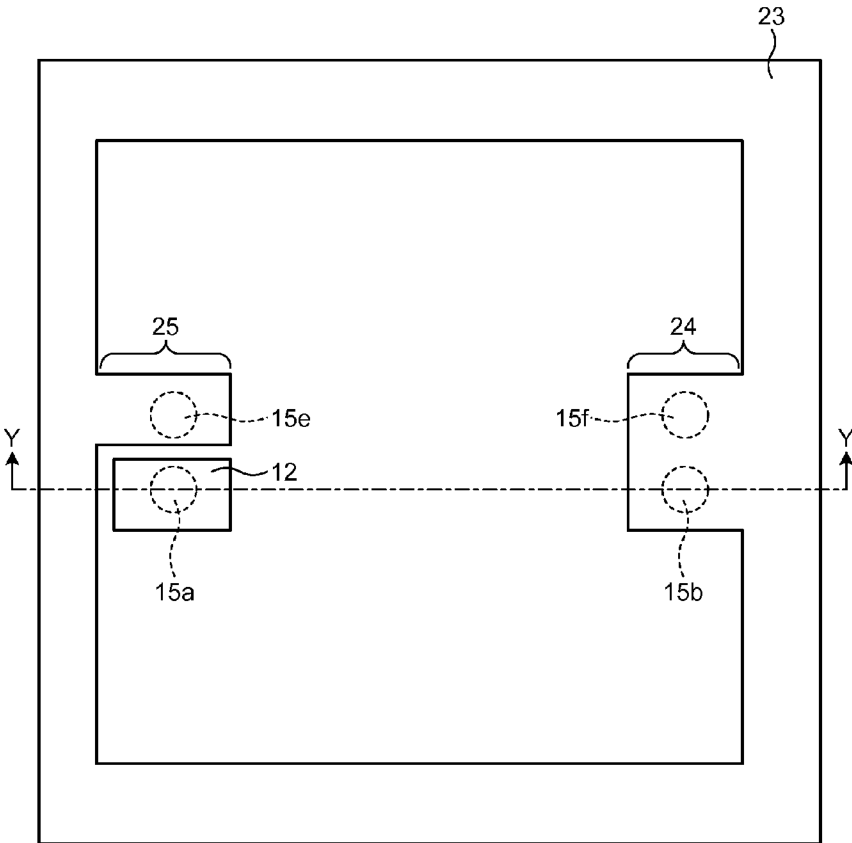


FIG.5A

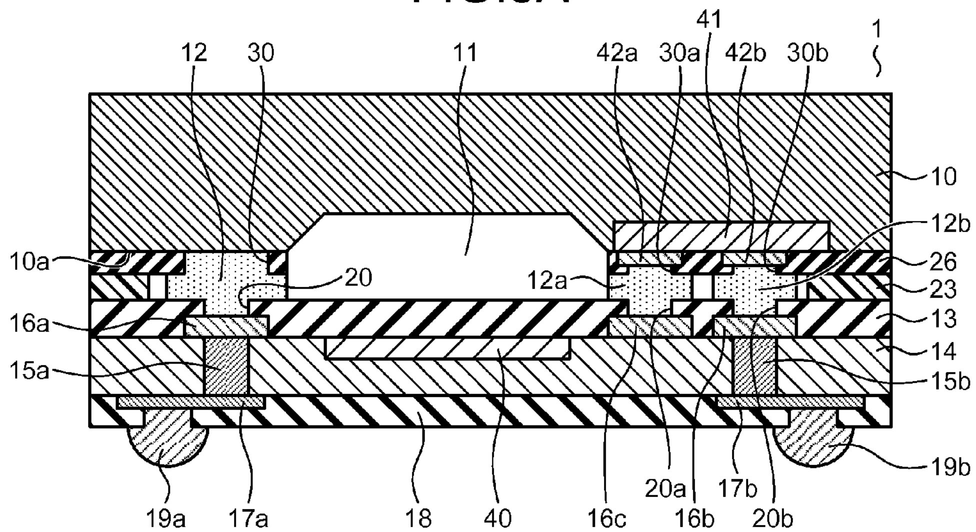
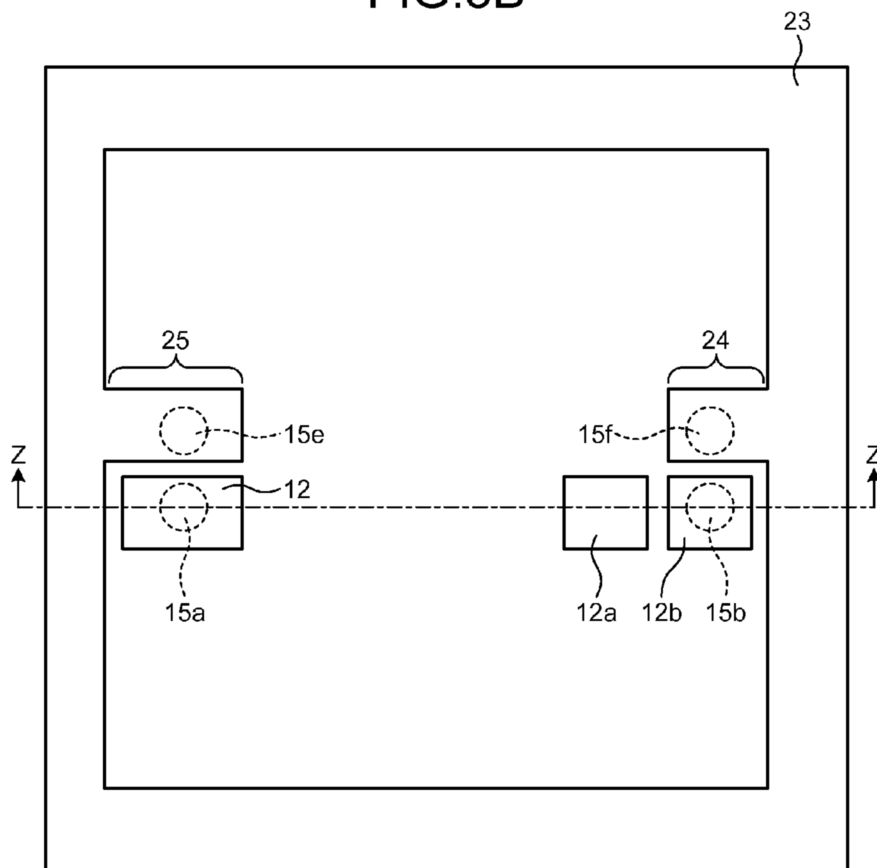


FIG.5B



SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from U.S. Provisional Application No. 61/827,960, filed on May 28, 2013; the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate to a semiconductor device using a wafer level packaging technology, and a method of manufacturing the same.

BACKGROUND

[0003] Conventionally, the demand for size reduction of a semiconductor device has increased along with the progress in manufacturing technology of the semiconductor device. One of technologies for meeting the demand for size reduction of the semiconductor device is a wafer level packaging technology. In the wafer level packaging technology, a semiconductor substrate where semiconductor elements have been formed at a wafer level is subjected to formation of wirings and electrodes at the wafer level, and then a surface of the semiconductor substrate is sealed with a predetermined cover and cut into a chip size through dicing, thereby providing individual semiconductor devices.

[0004] In the wafer level packaging technology, wirings formed on both main surfaces of the semiconductor substrate are connected to each other by a through silicon via (TSV) with which a through hole provided for the semiconductor substrate is filled. In the formation of the through hole, pressure applied to the wiring formed on the surface of the semiconductor substrate might result in a trouble of wiring separation or breakage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a schematic sectional view of a semiconductor device according to a first embodiment.

[0006] FIGS. **2**A and **2**B are diagrams for describing a positional relation between TSVs and a bonding member for bonding a semiconductor substrate and a conductive cover.

[0007] FIGS. **3**A to **3**D are diagrams for partially describing an example of a method of manufacturing a semiconductor device according to the first embodiment.

[0008] FIGS. **4**A and **4**B are a schematic sectional view of a semiconductor device according to a second embodiment and a diagram for describing a positional relation between the bonding member and the TSVs.

[0009] FIGS. **5**A and **5**B are a schematic sectional view of a semiconductor device according to a third embodiment and a diagram for describing a positional relation between the bonding member and the TSVs.

DETAILED DESCRIPTION

[0010] In general, according to one embodiment, a semiconductor device includes a semiconductor substrate having a first main surface and a second main surface and including a predetermined element formed on the first main surface and a plurality of TSVs configured to electrically connect a plurality of wirings formed on the first main surface to a plurality of electrodes correspondingly formed on the second main surface. The semiconductor device also includes a conductive cover which covers the first main surface of the semiconductor substrate, and a conductive bonding member which bonds the conductive cover and one wiring of the wirings formed on the first main surface of the semiconductor substrate to each other.

[0011] Exemplary embodiments of a semiconductor device and a method of manufacturing the same will be explained below in detail with reference to the accompanying drawings. The present invention is not limited to the following embodiments.

[0012] FIG. **1** is a schematic sectional view of a semiconductor device according to a first embodiment. A semiconductor device **1** of this embodiment includes a semiconductor substrate **14** provided with a predetermined active element **40**. In-chip wirings (**16***a* and **16***b*) are formed on a first main surface of the semiconductor substrate **14**. The in-chip wirings (**16***a* and **16***b*) are electrically connected to the active element **40**, for example. The first main surface of the semiconductor substrate **14** is provided with a passivation film **13** including a silicon nitride film, for example. On a second main surface of the semiconductor substrate **14**, specifically on a back surface, back wirings (**17***a* and **17***b*) are formed. The in-chip wirings (**16***a* and **16***b*) and the corresponding back wirings (**17***a* and **17***b*) are connected to each other by TSVs (**15***a* and **15***b*) provided for the semiconductor substrate **14**, respectively.

[0013] A passivation film **18** is formed on the second main surface of the semiconductor substrate **14**. The passivation film **18** is formed using, for example, a silicon nitride film. The back wirings (**17***a* and **17***b*) are connected to solder balls (**19***a* and **19***b*) via predetermined openings provided for the passivation film **18**. The solder balls (**19***a* and **19***b*) form external electrodes of the semiconductor device **1**. A conductive bonding member **12** is formed on the first main surface side of the semiconductor substrate **14**. For the conductive bonding member **12**, for example, Au—Sn alloy, Ag—Sn alloy, Cu—Sn alloy, Ag paste, or the like is used. The in-chip wiring **16***a* is electrically connected to the conductive bonding member **12** via an opening **20** provided for the passivation film **13**. To the solder ball **19***a* electrically connected to the conductive bonding member **12**, a ground potential is applied when the semiconductor device **1** is in operation (hereinafter referred to as operation time).

[0014] The first main surface side of the semiconductor substrate **14** is covered with a conductive cover **10**. As the conductive cover **10**, for example, a silicon substrate doped with boron is used. The conductive cover **10** is provided with a concave portion **11** facing the first main surface side of the semiconductor substrate **14**. With the thickness of the bonding member **12** and the concave portion **11** provided for the conductive cover **10**, a hollow portion is formed between the semiconductor substrate **14** and the conductive cover **10**. In this hollow portion, another element (not shown) can be disposed. For example, a passive element such as a coil or a capacitor, or an active element such as an Integrated Circuit (IC) chip, can be disposed. The conductive cover **10** and the semiconductor substrate **14** are bonded to each other with the conductive bonding member **12**. A bonding unit **10***a* for forming the periphery of the concave portion **11** of the conductive cover **10** is bonded to the semiconductor substrate **14** with the bonding member **12** on the semiconductor substrate **14**. Note that when another element (not shown) is disposed in the

cal Vapor Deposition) on the back surface of the semiconductor substrate **14**. Then, the protective film at the bottom of the through hole **30**, specifically, on the surface of the in-chip wirings (**16***a* and **16***b*) on the through hole side is selectively removed by RIE. Next, a seed layer (not shown) including Cu, for example, is formed on the entire back surface of the semiconductor substrate **14** by sputtering. A resist film (not shown) is formed on the seed layer and a predetermined patterning step is performed, thereby forming openings (not shown) corresponding to the through holes **30**. Subsequently, a Cu plating step is performed to fill the through holes **30** with Cu, thereby forming the TSVs (**15***a*, **15***b*, **15***c*, and **15***d*). Note that as for the filling of the through holes **30** with Cu, the through holes **30** are not necessarily filled completely. The TSVs (**15***a*, **15***b*, **15***c*, and **15***d*) may merely fulfill the function of electrically connecting the in-chip wirings (**16***a* and **16***b*) formed on the first main surface side of the semiconductor substrate **14** to the back wirings formed on the second main surface side. Even though the incomplete filling of the through hole **30** with the TSV generates the space inside the through hole **30**, the space can be filled by a subsequently performed wiring step on the second main surface side of the semiconductor substrate **14** or by the predetermined passivation film formed on the second main surface side of the semiconductor substrate **14**. Subsequently, the resist layer is separated and the Cu seed layer is selectively removed by etching.

[0024] Subsequently, the wiring step is performed on the second main surface side, specifically, the back side of the semiconductor substrate **14**. For example, the wiring step on the back side is performed as below. For example, a back wiring (not shown) including aluminum to be connected to the TSV is formed on the back side of the semiconductor substrate **14** in a photolithography step and an etching step. Subsequently, a passivation film (not shown) including, for example, silicon nitride is formed on the second main surface of the semiconductor substrate **14**. The passivation film is subjected to predetermined patterning, thereby forming a predetermined opening (not shown) for exposing a part of a surface of the back wiring. A solder is mounted on the predetermined opening provided for the passivation film, and a reflow step is performed to form a solder ball (not shown). Note that the back wiring may be formed by extending a Cu layer, which forms the TSV, onto the second main surface of the semiconductor substrate **14**. Finally, a dicing step is performed to divide the substrate into individual semiconductor devices. The dicing is performed at positions indicated by arrows (**50** and **51**) in FIG. **3**D.

[0025] As thus described, the passivation film **13**, the bonding member **12**, and the conductive cover **10** are formed over the in-chip wirings (**16***a* and **16***b*) having the through holes **30**. In other words, no space is formed between the in-chip wirings (**16***a* and **16***b*) and the conductive cover **10**. Therefore, it is possible to prevent the in-chip wirings (**16***a* and **16***b*) from being separated or broken by pressure applied in a washing step or the like when the through holes **30** are formed through the semiconductor substrate **14**.

[0026] FIGS. **4**A and **4**B are a schematic sectional view of the semiconductor device according to a second embodiment, and a diagram for describing the positional relation between the bonding member and the TSVs. The components corresponding to those in the above embodiment are denoted with the same reference symbols, and the description is omitted. FIG. **4**A is a schematic sectional view of the semiconductor device **1**. FIG. **4**B is a plan view of the pattern shape of bonding members (**12** and **23**) provided on the main surface of the semiconductor substrate **14**. FIG. **4**A schematically illustrates the sectional structure of the semiconductor device **1** along an alternate long and short dash line Y-Y of FIG. **4**B.

[0027] In this embodiment, except a part, the bonding member for bonding the conductive cover **10** and the semiconductor substrate **14** is constituted by an insulating bonding member **23**. As illustrated in FIG. **4**B, the insulating bonding member **23** includes a projection portion **24** and a projection portion **25** projecting inward from the periphery. The projection portion **24** is disposed extending over the TSVs (**15***b* and **15***f*). The projection portion **25** is disposed extending over the TSV **15***e*. The conductive bonding member **12** is disposed on the in-chip wiring **16***a* electrically connected to the solder ball **19***a* to which the ground potential is applied during the operation time. The in-chip wiring **16***a* is bonded to the conductive cover **10** with the conductive bonding member **12**. For the conductive bonding member **12**, for example, Au—Sn alloy, Ag—Sn alloy, Cu—Sn alloy, Ag paste, or the like is used. For the insulating bonding member **23**, a photosensitive adhesive resin is used, for example. The photosensitive adhesive resin is formed on the passivation film **13** and predetermined patterning is performed, thereby providing the bonding member **23**.

[0028] In this embodiment, the conductive bonding member **12** is provided just on the TSV **15***a* connected to the solder ball **19***a* to which the ground potential is applied during the operation time. The ground potential applied to the solder ball **19***a* is supplied to the conductive cover **10** via the TSV **15***a*, the in-chip wiring **16***a*, and moreover the conductive bonding member **12**. With this configuration, the conductive cover **10** exhibits the electromagnetic shielding effect. Over the other TSVs (**15***e* and **15***f*) including the TSV **15***b*, the projection portion **24** and the projection portion **25** of the insulating bonding member **23** extending inward from the periphery are provided. In this embodiment, the conductive cover **10** and the semiconductor substrate **14** are bonded to each other mainly with the insulating bonding member **23** provided for the periphery of the semiconductor substrate **14**. The amount of usage of the conductive bonding member **12** containing a noble metal such as Au or Ag can be reduced, thereby reducing the manufacturing cost of the semiconductor device. Moreover, since the conductive bonding member **12** is not exposed during the dicing, the outflow of the bonding member **12** can be prevented.

[0029] FIGS. **5**A and **5**B are a schematic sectional view of the semiconductor device according to a third embodiment, and a diagram for describing the positional relation between the bonding member and the TSVs. The components corresponding to those in the above embodiments are denoted with the same reference symbols, and the description is omitted. FIG. **5**A is a schematic sectional view of the semiconductor device **1**. FIG. **5**B is a plan view of the pattern shape of bonding members (**12**, **12***a*, **12***b*, and **23**) provided on the main surface of the semiconductor substrate **14**. FIG. **5**A schematically illustrates the sectional structure of the semiconductor device **1** along an alternate long and short dash line Z-Z of FIG. **5**B.

[0030] In this embodiment, the conductive cover **10** is also provided with a predetermined active element **41**. The active element **41** can be formed by introducing a predetermined impurity to the conductive cover **10** including a silicon substrate in a manner similar to the semiconductor substrate **14**.

On the active element **41** of the conductive cover **10**, in-chip wirings (**42***a* and **42***b*) are formed. Each of the in-chip wirings (**42***a* and **42***b*) is electrically connected to the active element **41**. The in-chip wiring **42***a* is electrically bonded to the conductive bonding member **12***a* via an opening **30***a* provided for a passivation film **26** including, for example, silicon nitride formed on a surface of the conductive cover **10**. The conductive bonding member **12***a* is electrically connected to an in-chip wiring **16***c* on the semiconductor substrate **14** side via an opening **20***a* provided for the passivation film **13** on the semiconductor substrate **14**. By electrically connecting the in-chip wiring **42***a* on the conductive cover **10** side and the in-chip wiring **16***c* on the semiconductor substrate **14** side to each other, signal transmission and reception are allowed between the active element **40** provided for the semiconductor substrate **14** and the active element **41** formed on the conductive cover **10** side.

[0031] The in-chip wiring **42***b* on the conductive cover **10** side is electrically connected to the in-chip wiring **16***b* on the semiconductor substrate **14** side via the conductive boding member **12***b*. For example, the in-chip wiring **16***b* on the semiconductor substrate **14** side is electrically connected to the active element **40**, and moreover electrically connected to the solder ball **19***b* serving as the external electrode. The signals supplied to the solder ball **19***b* can be supplied to the active element **40** provided for the semiconductor substrate **14** and the active element **41** provided for the conductive cover **10**.

[0032] The in-chip wiring **16***a* on the semiconductor substrate **14** side, which is electrically connected to the solder ball **19***a*, is bonded to the conductive bonding member **12**. The conductive bonding member **12** is bonded to the conductive cover **10** via the opening **30** provided for the passivation film **26**. By applying the ground potential, which is applied to the solder ball **19***a* during the operation time, to the conductive cover **10**, the conductive cover **10** exhibits the electromagnetic shielding effect.

[0033] According to this embodiment, the active element **41** is also provided for the conductive cover **10** including the silicon substrate. The conductive cover **10** is effectively used as the substrate forming the active element **41**. The conductive bonding members (**12**, **12***a*, and **12***b*) provided between the semiconductor substrate **14** and the conductive cover **10** are used as the bonding members between the semiconductor substrate **14** and the conductive cover **10**, and each have a function as a wiring between the active element **40** provided for the semiconductor substrate and the active element **41** provided for the conductive cover **10**.

[0034] In the manufacture of the semiconductor device **1** of this embodiment, for example, the conductive cover **10** is formed which includes the active element **41**, the in-chip wirings (**42***a* and **42***b*), the concave portion **11**, the passivation film **26**, and the conductive bonding members (**12**, **12***a*, and **12***b*) partially filling the openings (**30**, **30***a*, and **30***b*) of the passivation film **26**. Similarly, the semiconductor substrate **14** is formed which includes the predetermined active element **40**, the in-chip wirings (**16***a*, **16***b*, and **16***c*), the passivation film **13**, the conductive bonding members (**12**, **12***a*, and **12***b*), and the insulating bonding member **23** formed on the first main surface. The conductive cover **10** and the semiconductor substrate **14** are bonded to each other by thermal treatment. Next, the steps described with reference to FIG. **3**C and the subsequent drawings are performed, thereby manufacturing the semiconductor device **1**.

[0035] As the conductive cover **10**, a metal cover such as a Cu cover can be used. Although the conductive cover **10** having the concave portion is described in the embodiment, a conductive cover with a flat structure on the semiconductor substrate side can be used alternatively. In this case, the thickness of the bonding member for bonding the conductive cover and the semiconductor substrate forms the hollow portion between the conductive cover and the surface of the semiconductor substrate. Further, the solder ball electrically connected to the conductive cover via the TSV is not limited to the connection to the ground potential but may be a fixed potential. For example, the structure of applying a power source voltage VDD may be employed.

[0036] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a first main surface and a second main surface and including a predetermined element formed on the first main surface and a plurality of through silicon vias (TSVs) configured to electrically connect a plurality of wirings formed on the first main surface to a plurality of electrodes correspondingly formed on the second main surface;

a conductive cover configured to cover the first main surface of the semiconductor substrate; and

a conductive bonding member configured to bond the conductive cover and one wiring of the wirings formed on the first main surface of the semiconductor substrate to each other.

2. The semiconductor device according to claim **1**, wherein the bonding member surrounds a periphery on the first main surface of the semiconductor substrate and has a projection portion projecting inward from the periphery, and the projection portion of the bonding member extends over at least one of the TSVs provided for the semiconductor substrate.

3. The semiconductor device according to claim **2**, wherein during an operation time, a fixed potential is applied to the electrode among the electrodes formed on the second main surface, the electrode being electrically connected to the wiring bonded to the conductive cover with the conductive bonding member.

4. The semiconductor device according to claim **3**, wherein the fixed potential is a ground potential.

5. The semiconductor device according to claim **4**, wherein the conductive cover includes a silicon substrate doped with a predetermined impurity.

6. The semiconductor device according to claim **5**, wherein the conductive cover is provided with a predetermined concave portion facing the first main surface of the semiconductor substrate.

7. The semiconductor device according to claim **4**, wherein the conductive cover is made of metal.

8. The semiconductor device according to claim **1**, wherein during an operation time, a ground potential is applied to the electrode among the electrodes formed on the second main surface, the electrode being electrically connected to the wiring bonded to the conductive cover with the conductive bonding member.

9. The semiconductor device according to claim **8**, wherein the conductive cover includes a silicon substrate doped with a predetermined impurity.

10. The semiconductor device according to claim **9**, wherein the conductive cover is provided with a predetermined concave portion facing the first main surface of the semiconductor substrate.

11. A method of manufacturing a semiconductor device, comprising:

a step of preparing a semiconductor substrate having a predetermined element and a first wiring on a first main surface side, and a conductive bonding member with a predetermined pattern shape provided on a passivation film formed on the first wiring;

a step of preparing a conductive cover configured to cover the first main surface of the semiconductor substrate;

a step of bonding the conductive cover and the semiconductor substrate to each other with the bonding member;

a step of grinding a second main surface side of the semiconductor substrate, thereby thinning the semiconductor substrate;

a step of forming a through hole reaching the first wiring from the second main surface side of the semiconductor substrate corresponding to a position of the first wiring; and

a step of filling the through hole with a conductive material.

12. The method for manufacturing a semiconductor device according to claim **11**, wherein a washing step of washing the through hole is performed prior to the step of filling the through hole with the conductive material.

13. The method for manufacturing a semiconductor device according to claim **12**, wherein the washing step includes a washing step in which pure water is used.

14. A semiconductor device comprising:

a semiconductor substrate having a first main surface and a second main surface and including a predetermined element formed on the first main surface and a plurality of through silicon vias (TSVs) configured to electrically connect a plurality of wirings formed on the first main surface to a plurality of electrodes correspondingly formed on the second main surface;

a conductive cover configured to cover the first main surface of the semiconductor substrate;

an insulating bonding member provided between the conductive cover and the first main surface of the semiconductor substrate and surrounding a periphery on the first main surface of the semiconductor substrate; and

a conductive bonding member provided between the conductive cover and the wiring formed on the first main surface in a region surrounded by the insulating bonding member.

15. The semiconductor device according to claim **14**, wherein the conductive bonding member is bonded to one wiring of the wirings formed on the first main surface.

16. The semiconductor device according to claim **15**, wherein during an operation time, a ground potential is applied to the electrode among the electrodes formed on the second main surface, the electrode being electrically connected to the wiring bonded to the conductive cover with the conductive bonding member.

17. The semiconductor device according to claim **16**, wherein the conductive cover is provided with a predetermined concave portion facing the first main surface of the semiconductor substrate.

18. The semiconductor device according to claim **17**, wherein the conductive cover includes a silicon substrate doped with a predetermined impurity.

19. The semiconductor device according to claim **18**, wherein the conductive cover is provided with a predetermined active element.

20. The semiconductor device according to claim **19**, wherein a plurality of conductive bonding members is provided between the wirings formed on the first main surface and the conductive cover, and the predetermined element formed on the first main surface of the semiconductor substrate and the predetermined active element provided for the conductive cover are electrically connected to each other via one of the plurality of conductive bonding members.

* * * * *