US010461000B2

(12) **United States Patent**
Seddon et al.

(10) **Patent No.: US 10,461,000 B2**
(45) **Date of Patent: *Oct. 29, 2019**

(54) **SEMICONDUCTOR WAFER AND METHOD OF PROBE TESTING**

(71) Applicant: **SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC**, Phoenix, AZ (US)

(72) Inventors: **Michael J. Seddon**, Gilbert, AZ (US); **Heng Chen Lee**, Seremban (MY)

(73) Assignee: **SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC**, Phoenix, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/907,931**

(22) Filed: **Feb. 28, 2018**

(65) **Prior Publication Data**

US 2018/0190552 A1 Jul. 5, 2018

Related U.S. Application Data

(63) Continuation-in-part of application No. 15/704,246, filed on Sep. 14, 2017, now Pat. No. 10,170,381,
(Continued)

(51) **Int. Cl.**
H01L 23/58 (2006.01)
H01L 29/10 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 22/34*** (2013.01); ***H01L 21/6836*** (2013.01); ***H01L 22/12*** (2013.01);
(Continued)

(58) **Field of Classification Search**
USPC 257/48, E23.179, E21.521, E21.524; 438/113, 15
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2010/0194423 A1* 8/2010 Tago G01R 31/2889 324/762.01
2013/0076384 A1* 3/2013 Chang G01R 31/318513 324/754.01

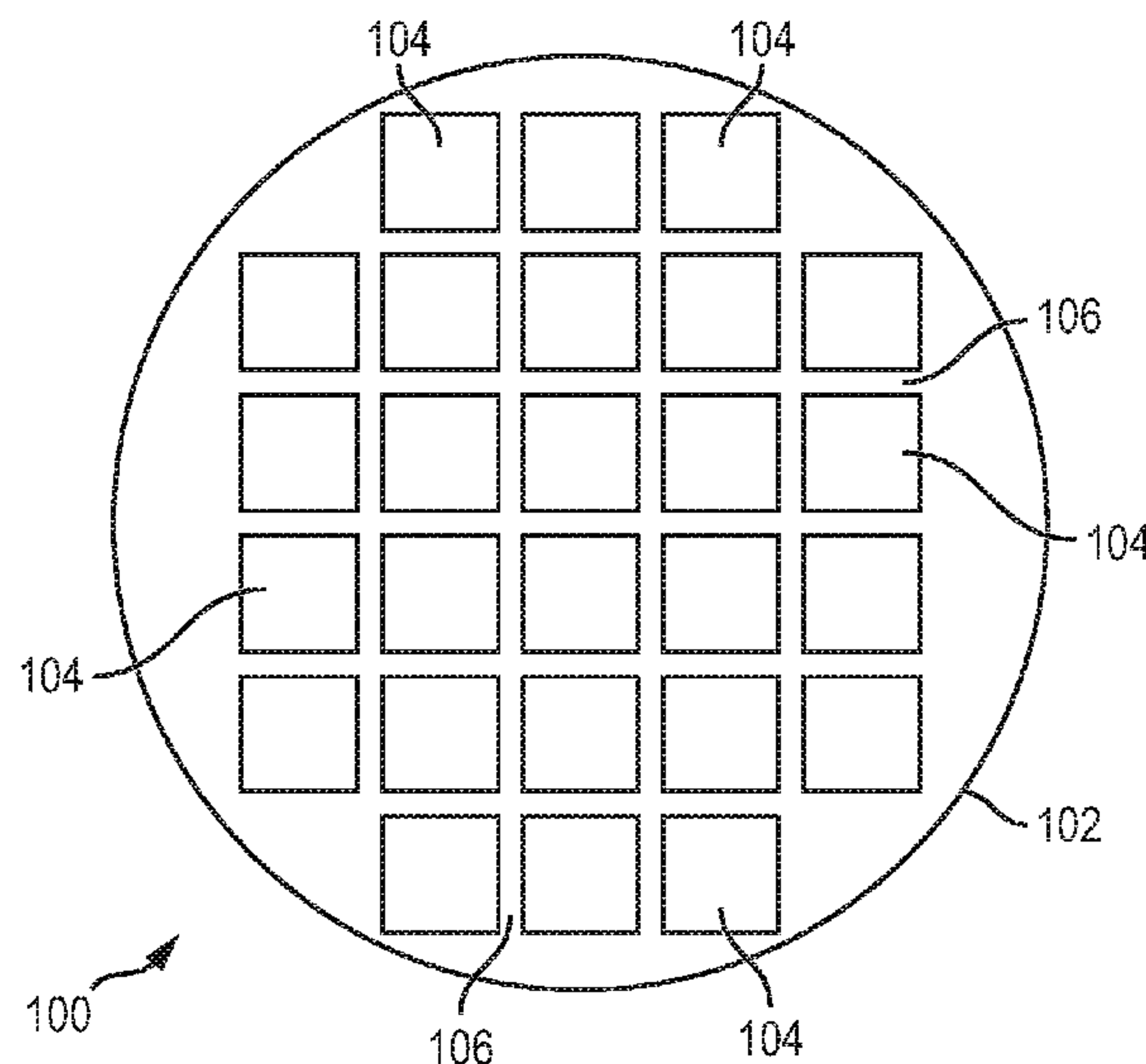
(Continued)

Primary Examiner — Niki H Nguyen
(74) *Attorney, Agent, or Firm* — Adam R. Stephenson, LTD.

(57) **ABSTRACT**

A semiconductor test system has a wafer holder with a tape portion and one or more openings through the tape portion. A semiconductor wafer is mounted over the opening in the tape portion of the wafer holder with an electrical connection to the semiconductor wafer through the opening in the tape portion during probe test. A plurality of bumps can be formed on the semiconductor wafer. The semiconductor wafer can be a stacked semiconductor wafer. A conductive trace can be formed on the tape portion and the semiconductor wafer probe tested through the conductive trace. An active surface or non-active surface of the semiconductor wafer can be oriented toward the tape portion. The electrical connection to the semiconductor wafer through the opening in the tape portion can be a ground reference node. A conductive layer is formed over a non-active surface of the semiconductor wafer.

20 Claims, 14 Drawing Sheets



Related U.S. Application Data

which is a continuation of application No. 15/230,875, filed on Aug. 8, 2016, now Pat. No. 9,793,186.

(51) **Int. Cl.**
H01L 21/66 (2006.01)
H01L 21/683 (2006.01)
H01L 21/78 (2006.01)
H01L 21/304 (2006.01)
G01R 31/28 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 22/32*** (2013.01); *G01R 31/2865* (2013.01); *G01R 31/2886* (2013.01); *H01L 21/304* (2013.01); *H01L 21/78* (2013.01); *H01L 22/14* (2013.01); *H01L 2221/68304* (2013.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

2014/0051189 A1 2/2014 Kai-Jun
2014/0203829 A1 7/2014 Yamada
2014/0252641 A1* 9/2014 Lim H01L 23/3128 257/773
2015/0001709 A1* 1/2015 Bao H01L 23/49811 257/737
2015/0015288 A1* 1/2015 Ma G01R 1/06738 324/754.03

* cited by examiner

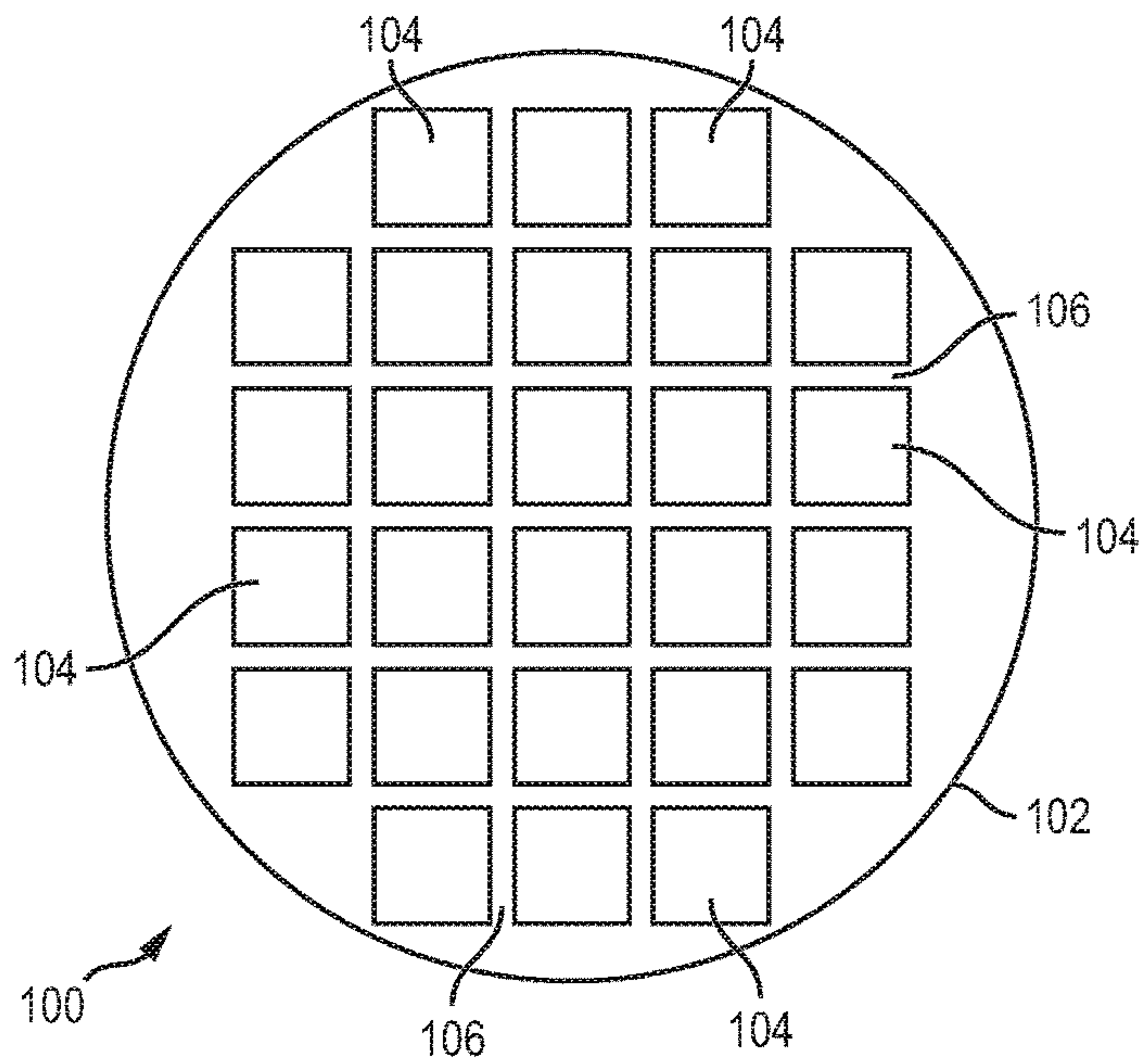


FIG. 1a

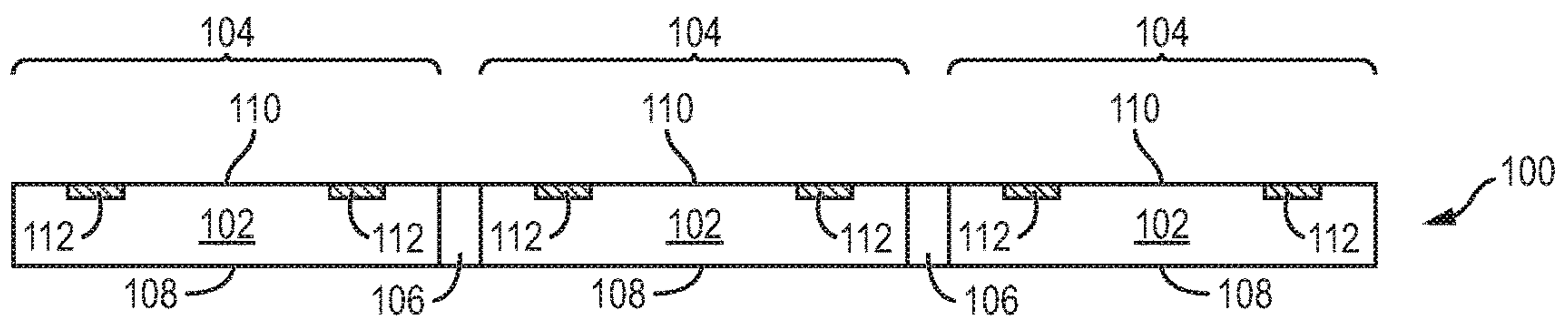


FIG. 1b

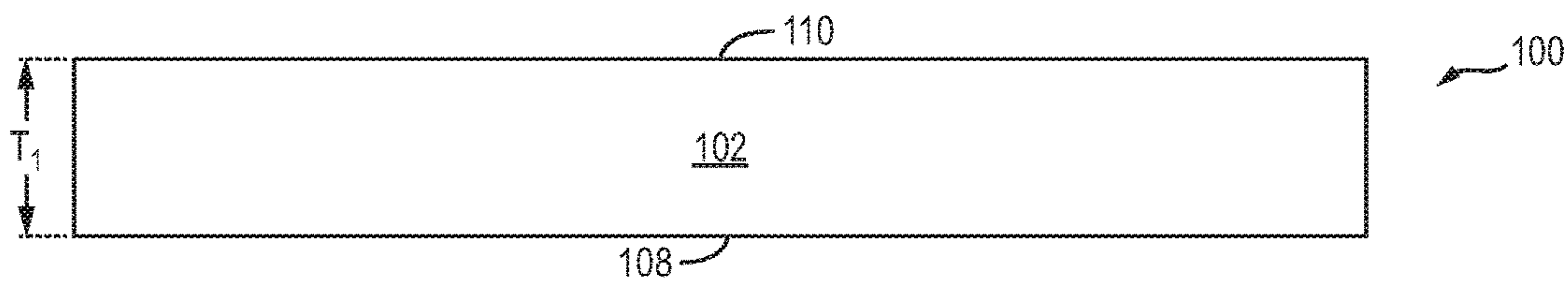


FIG. 2a

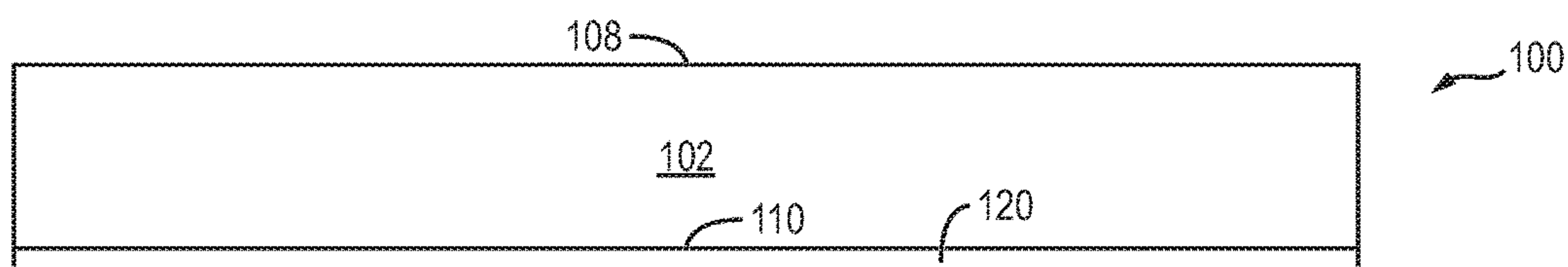


FIG. 2b

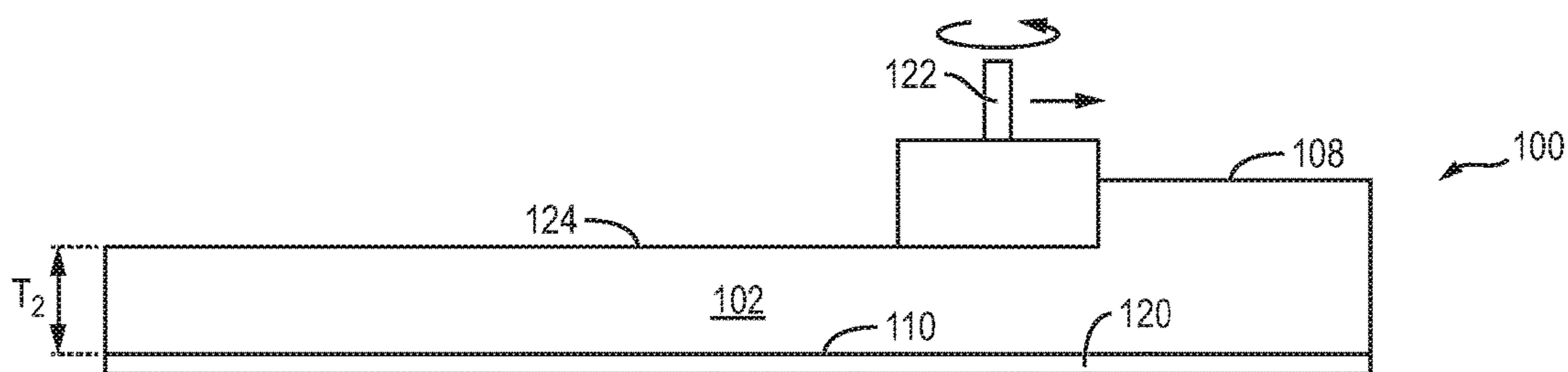


FIG. 2c

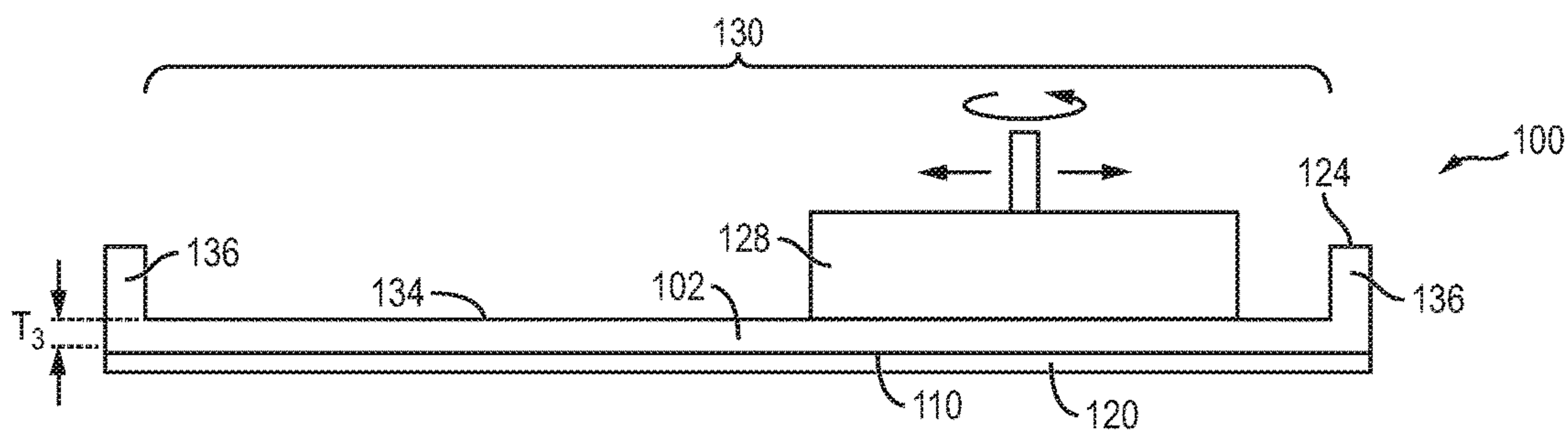


FIG. 2d

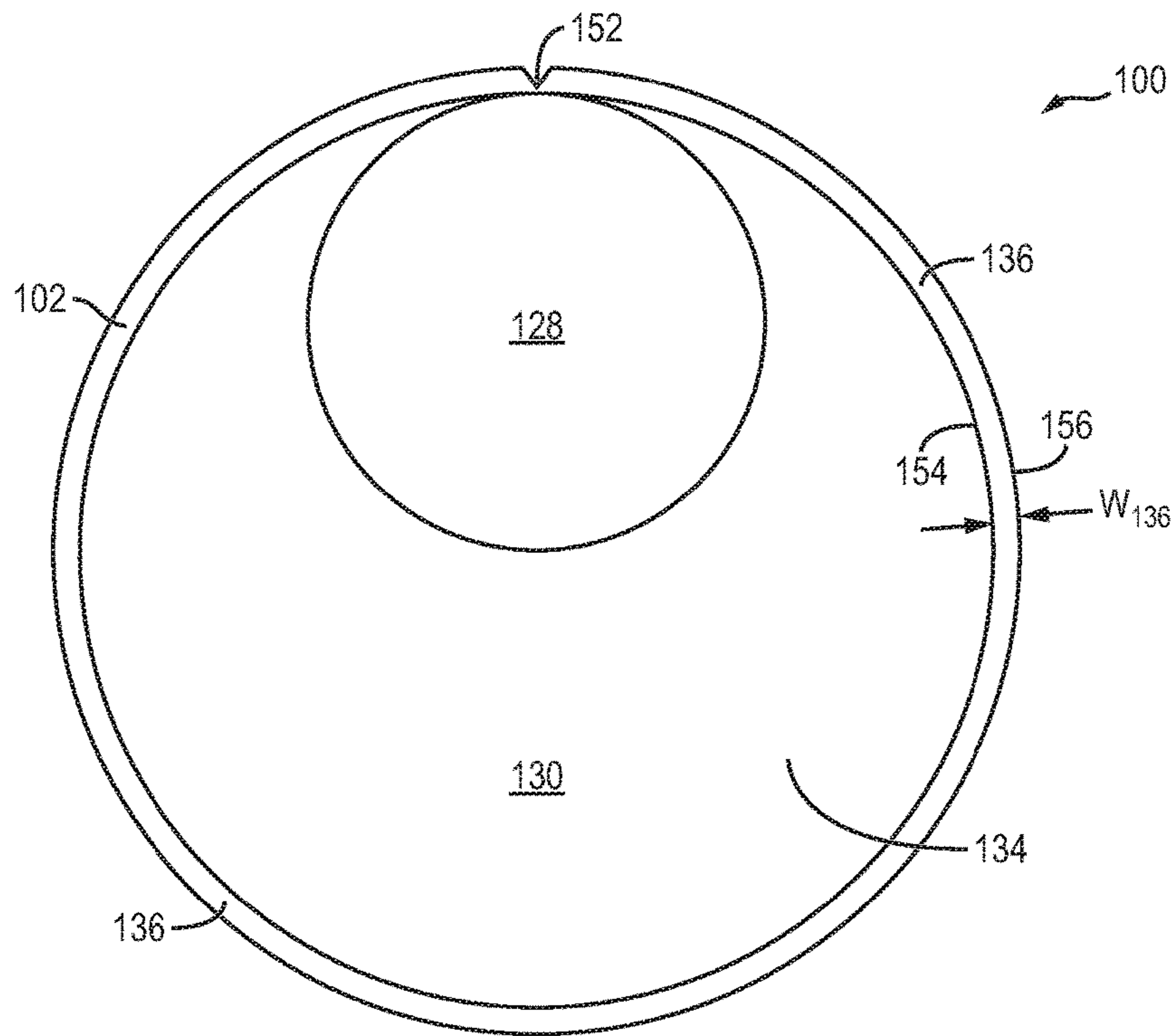


FIG. 2e

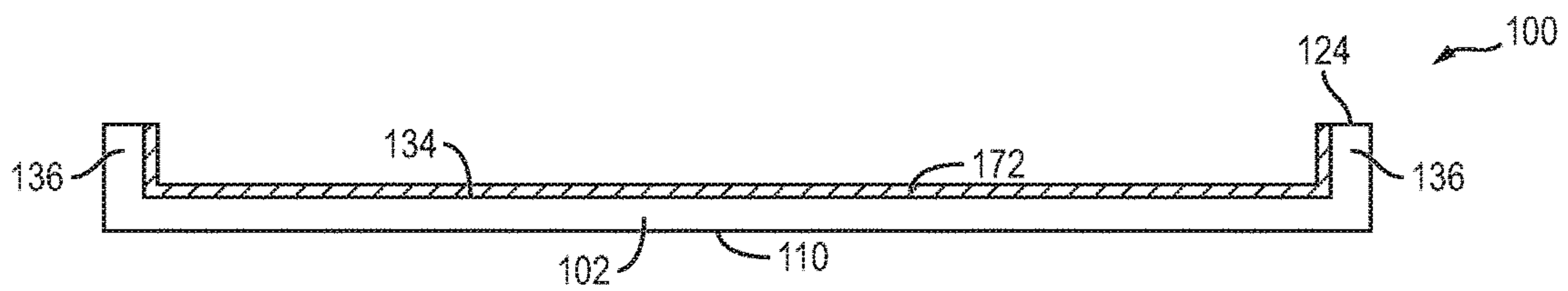


FIG. 2f

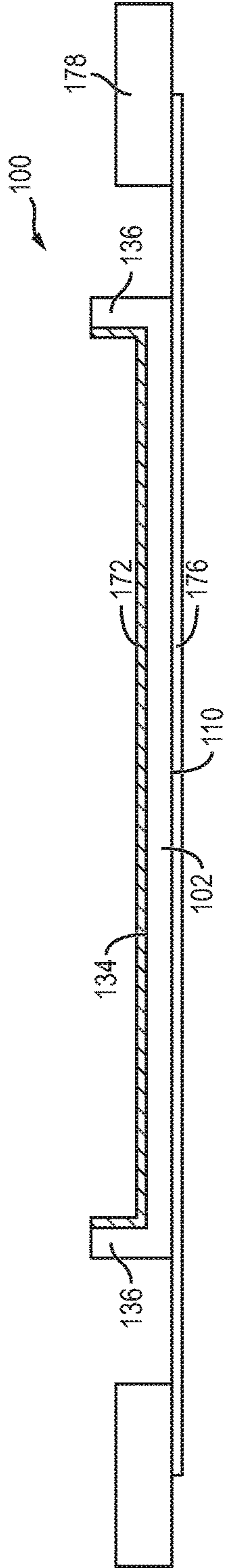


FIG. 2g

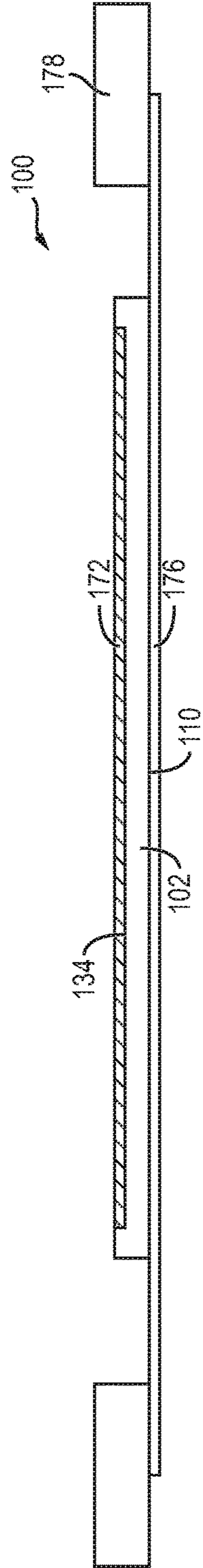


FIG. 2h

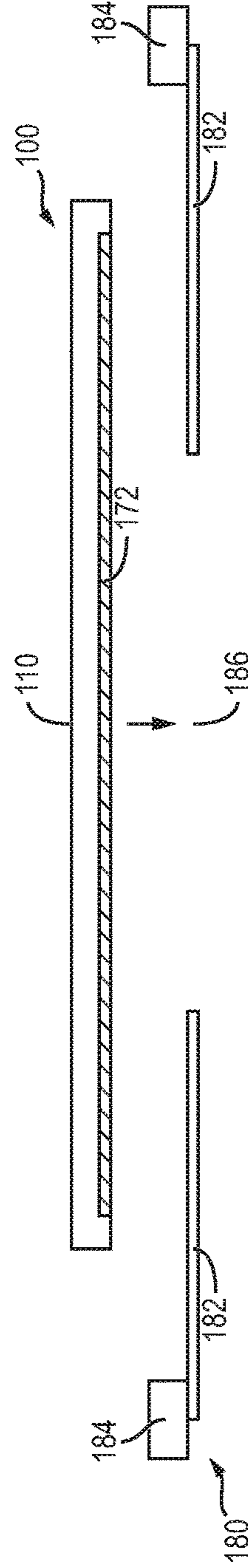


FIG. 3a

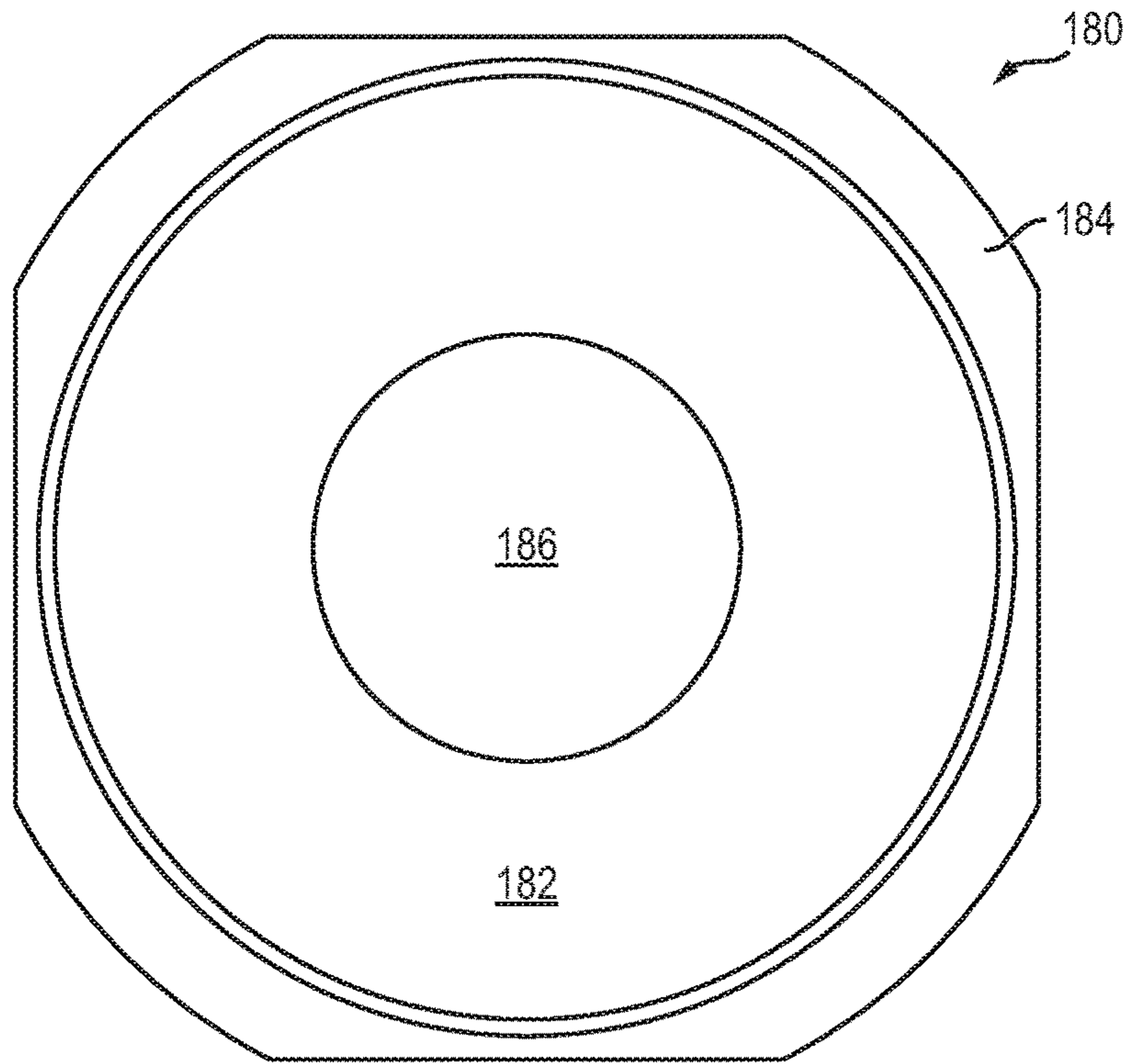


FIG. 3b

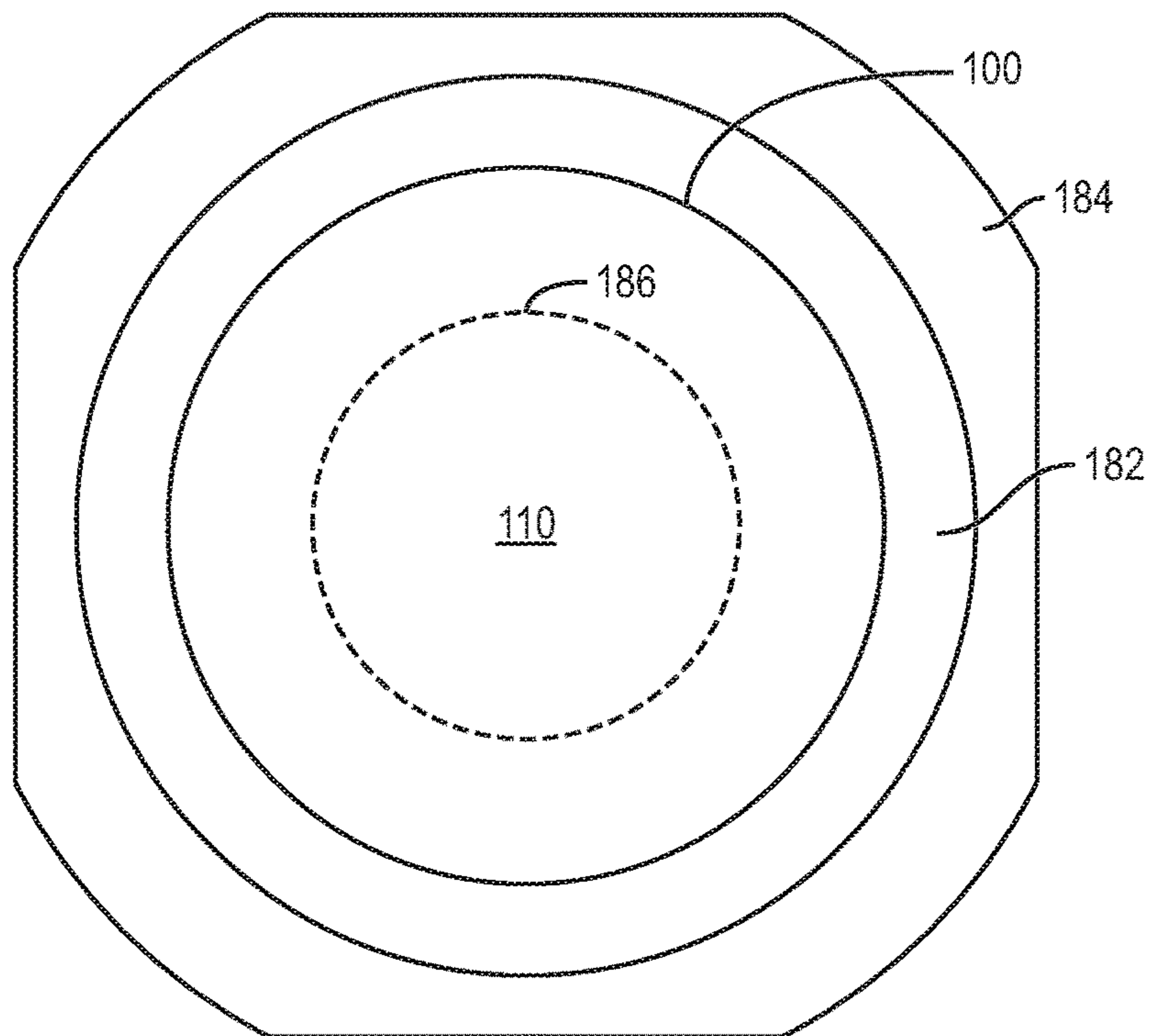


FIG. 3c

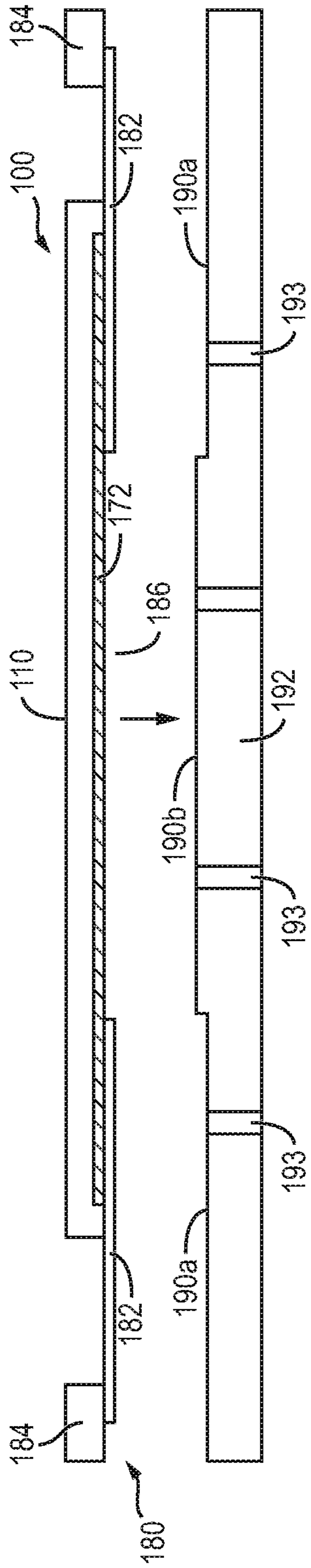


FIG. 3d

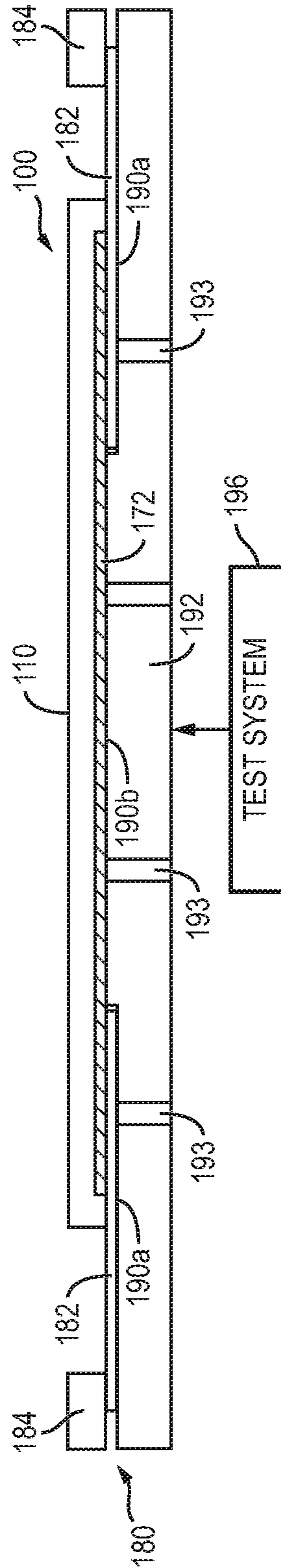


FIG. 3e

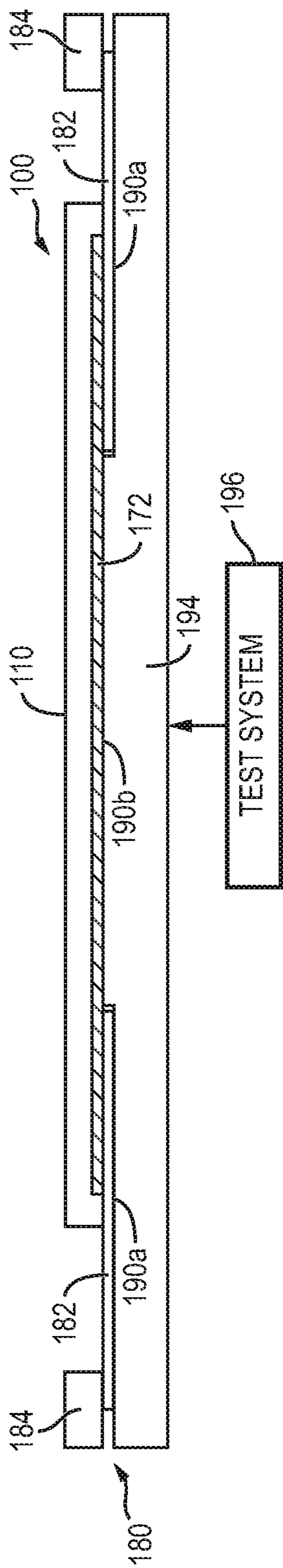


FIG. 3f

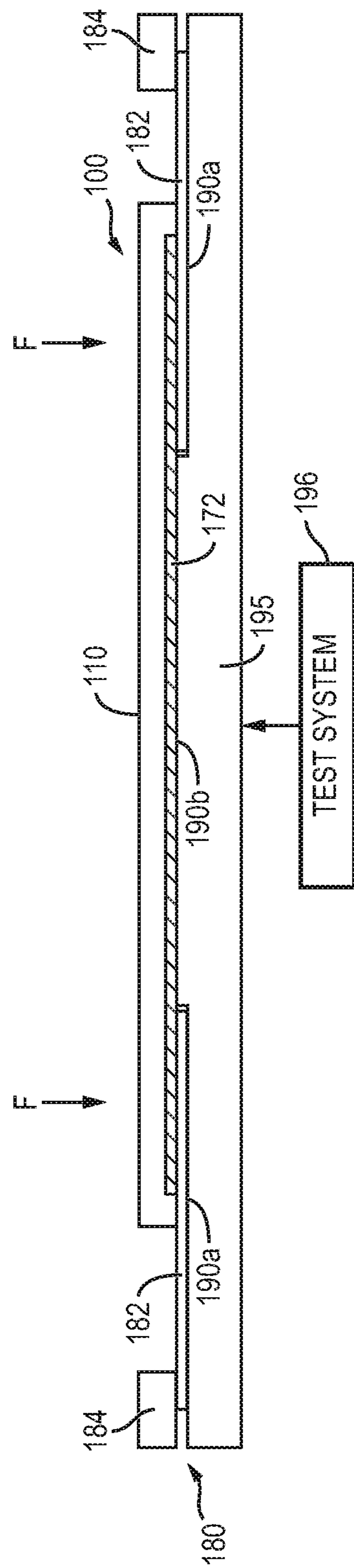


FIG. 3g

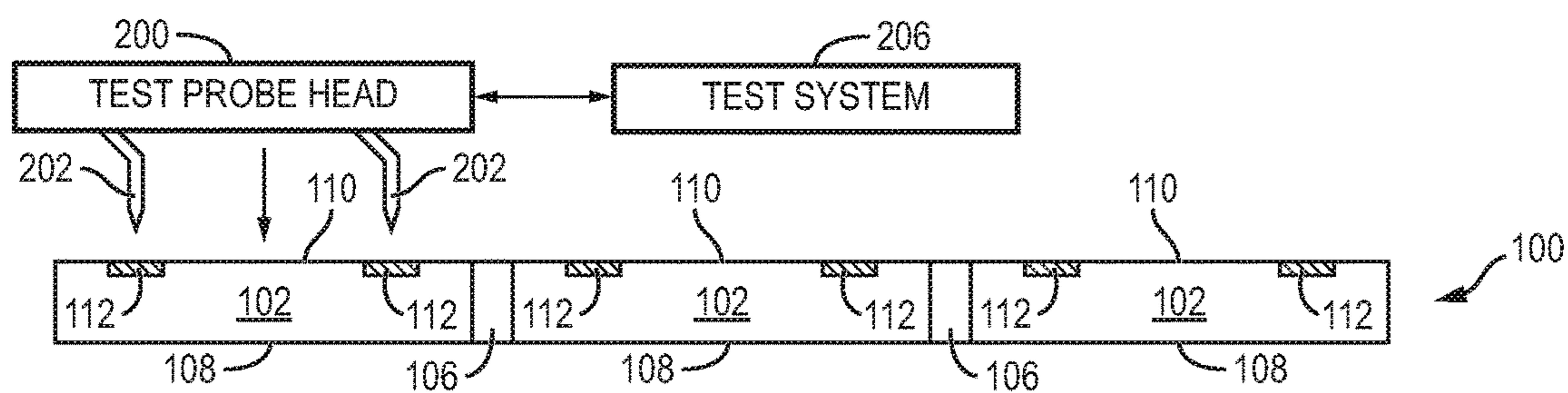


FIG. 3h

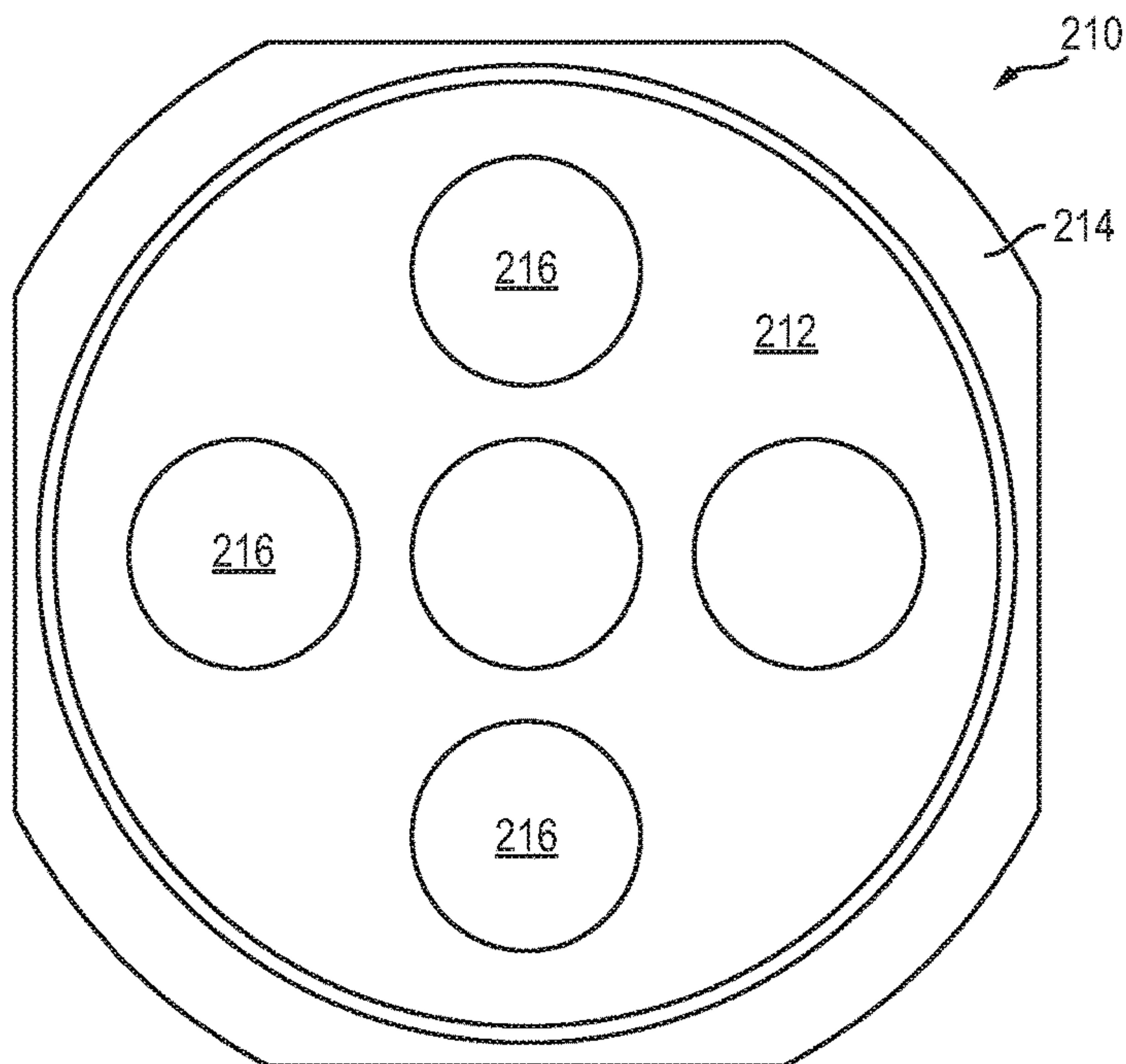


FIG. 3i

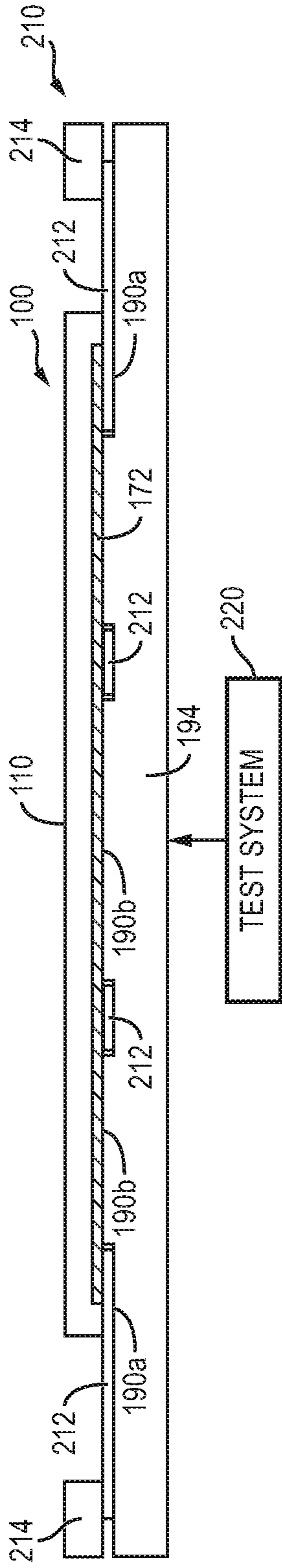


FIG. 3j

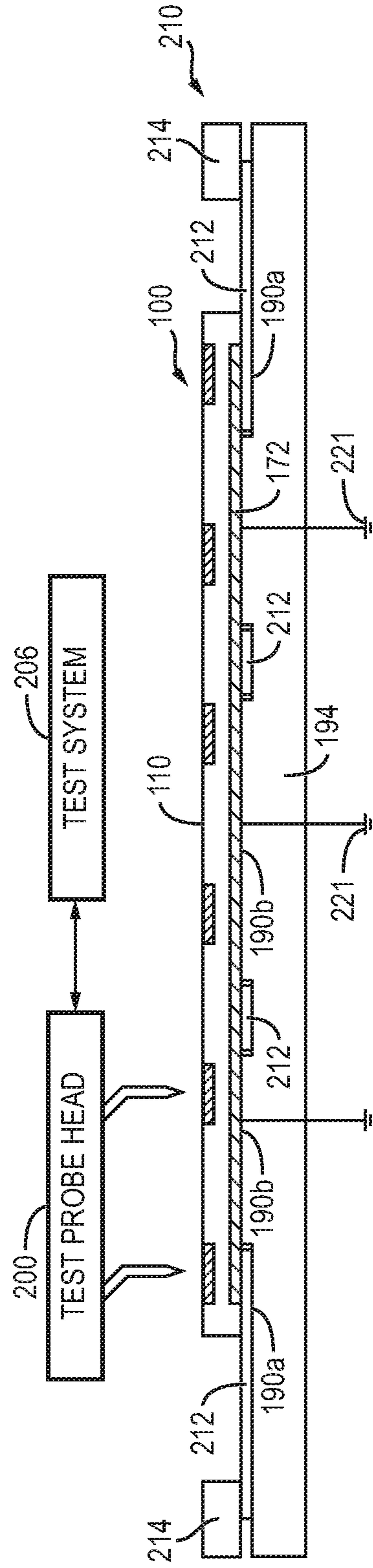


FIG. 3k

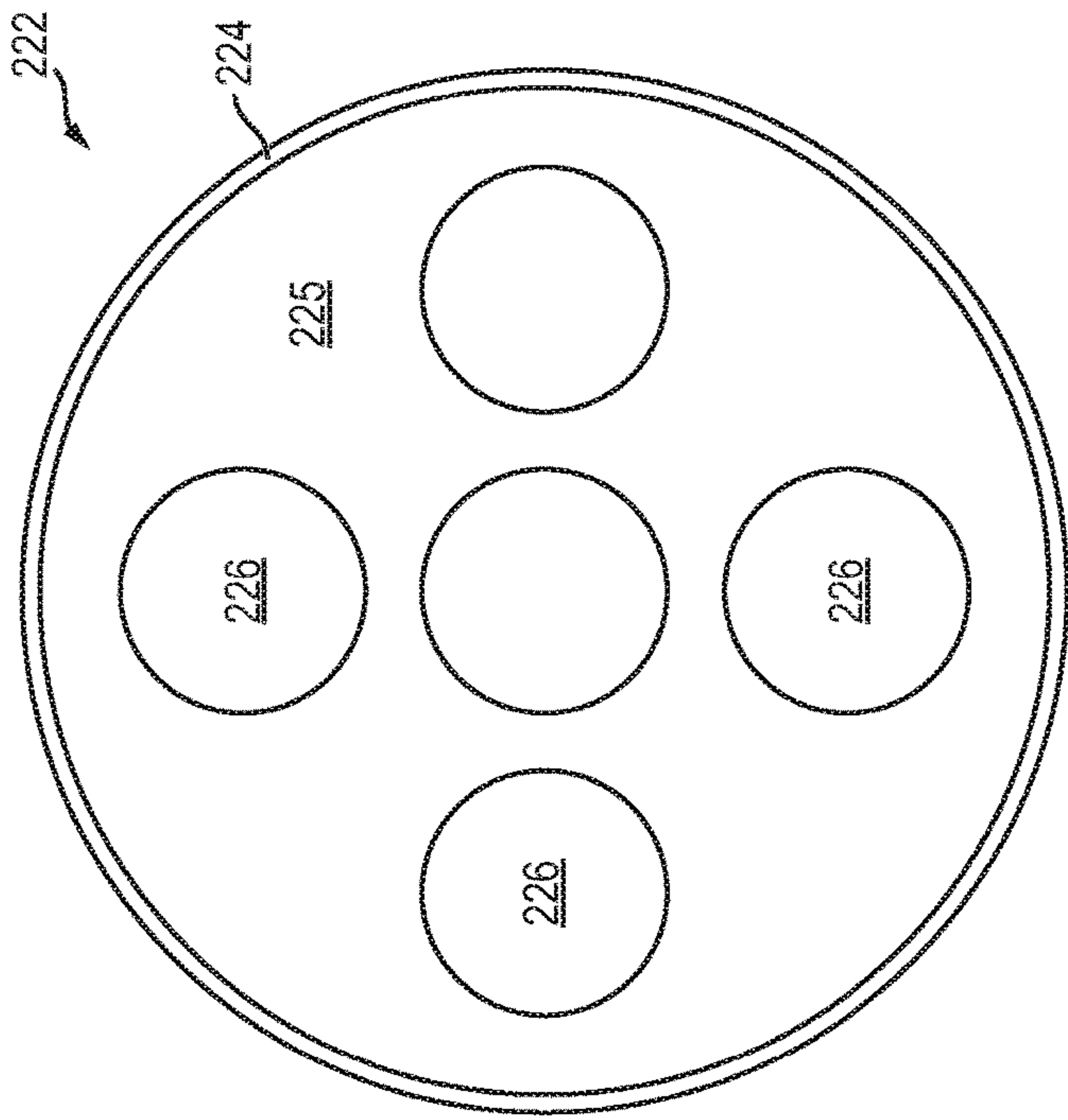


FIG. 3l

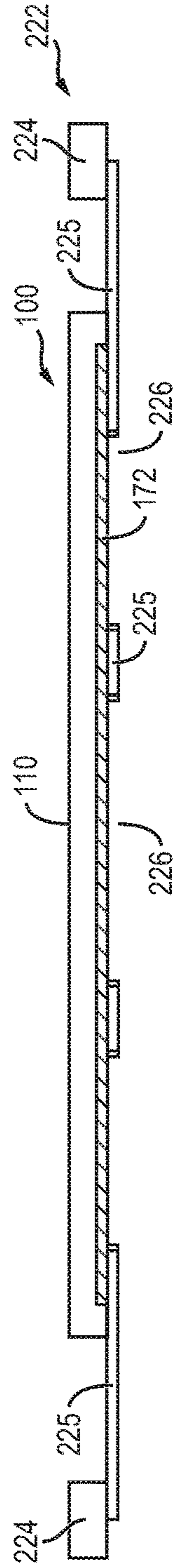


FIG. 3m

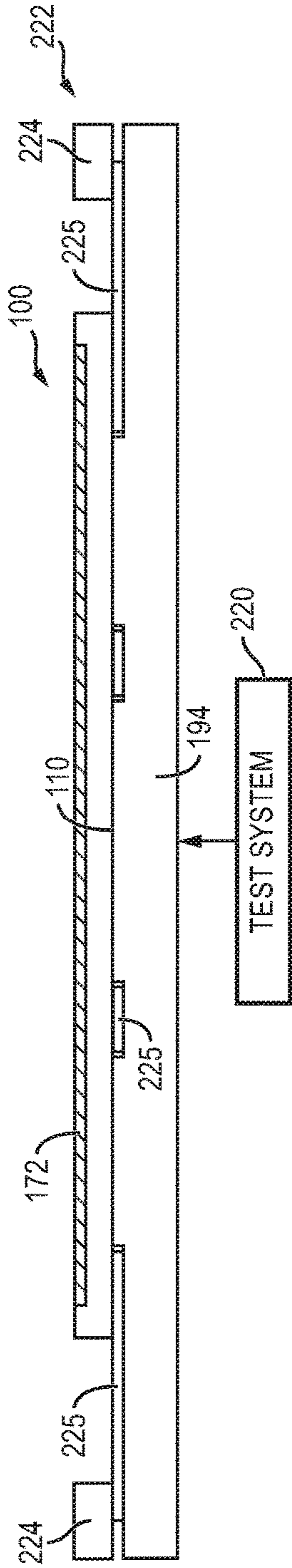


FIG. 3n

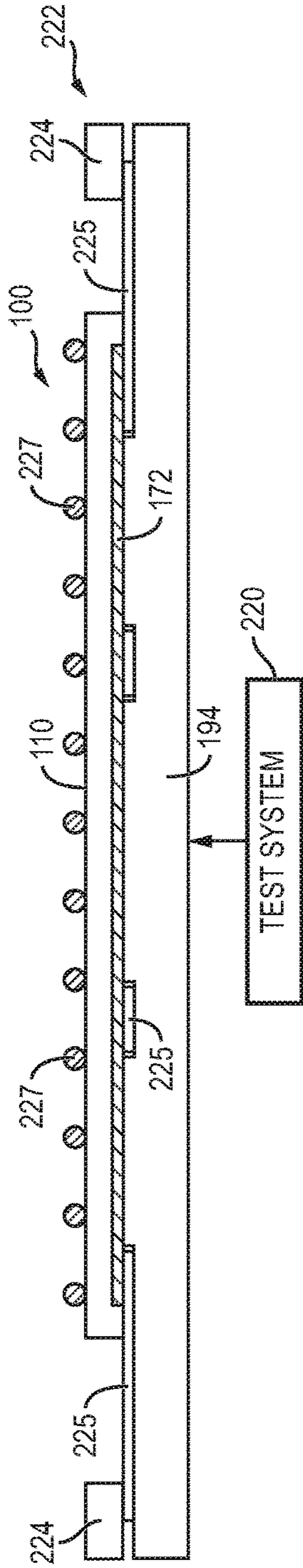


FIG. 3o

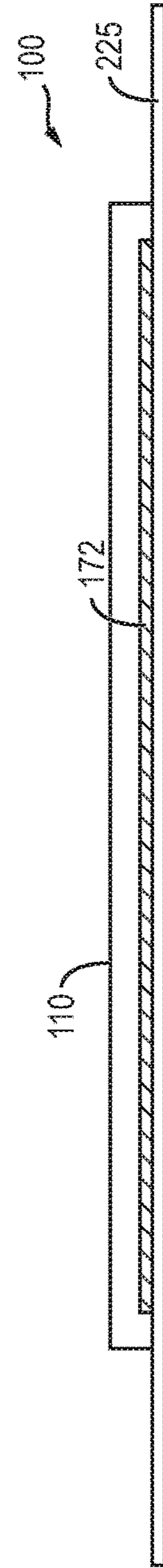


FIG. 3p

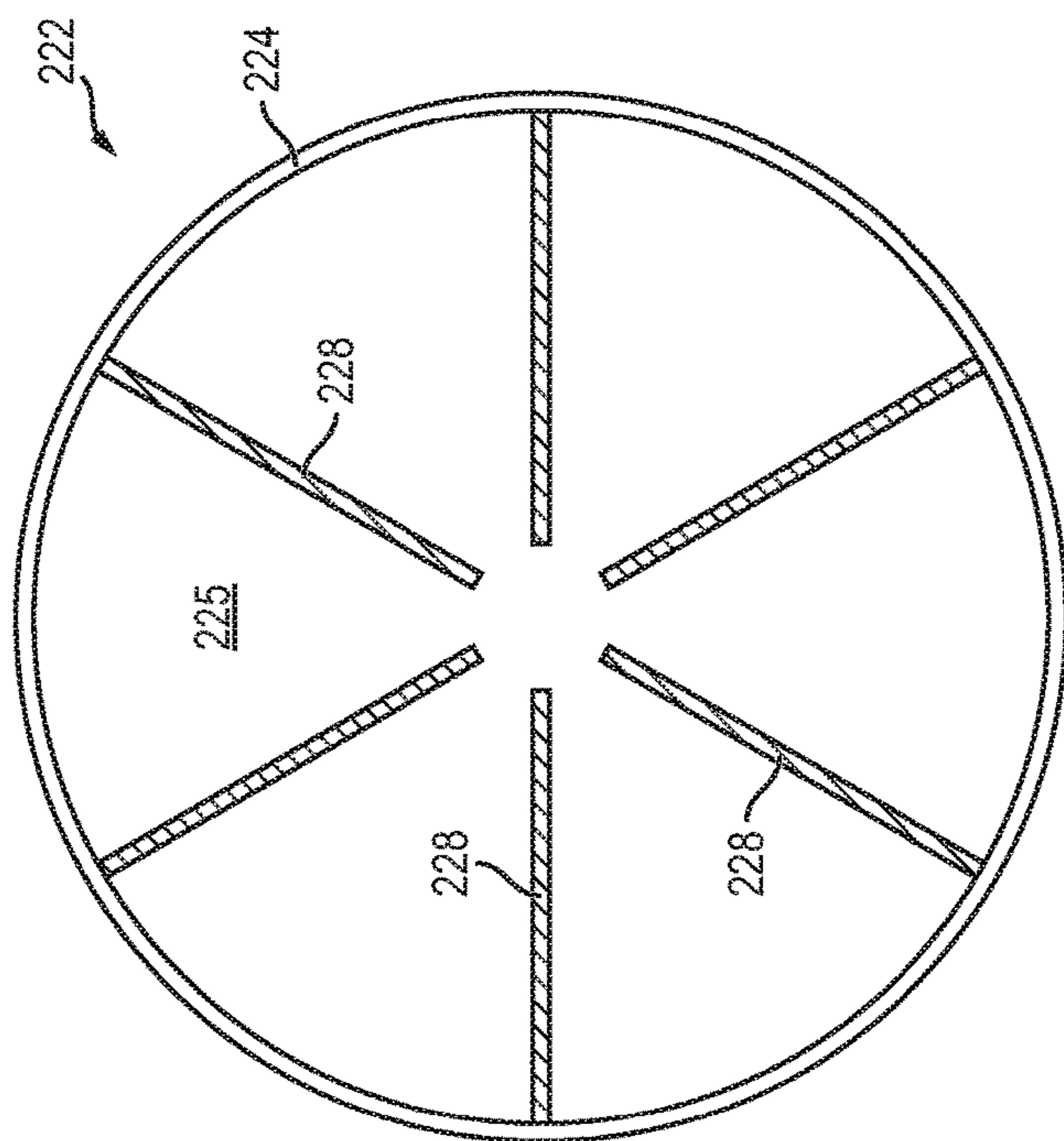


FIG. 3q

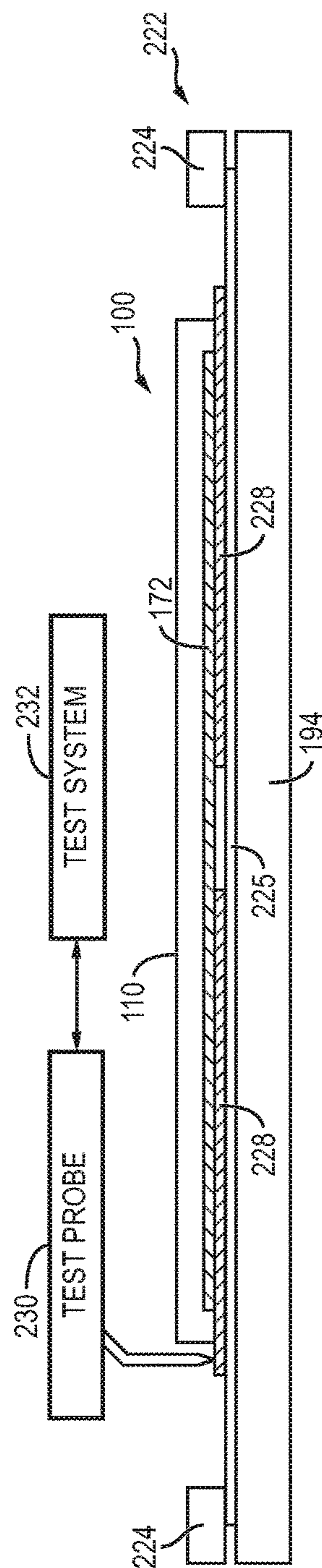


FIG. 3r

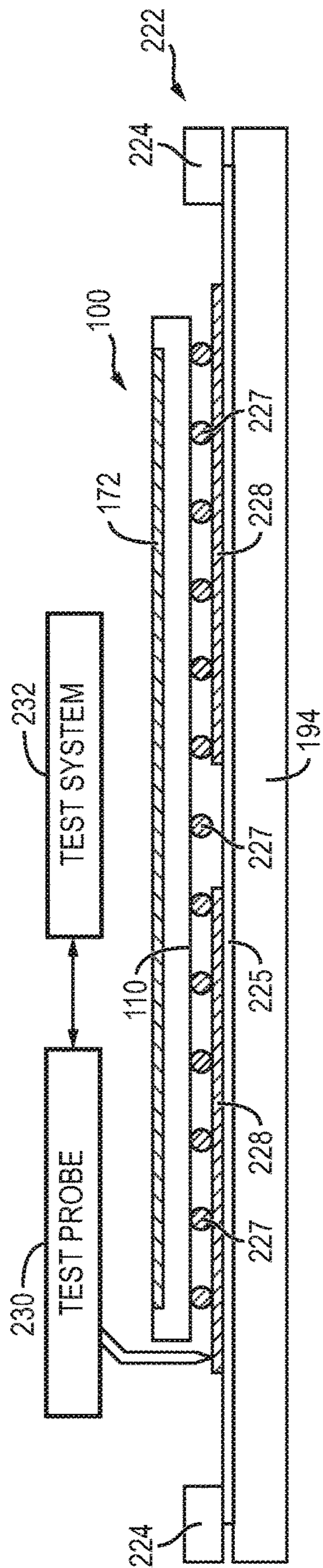


FIG. 3s

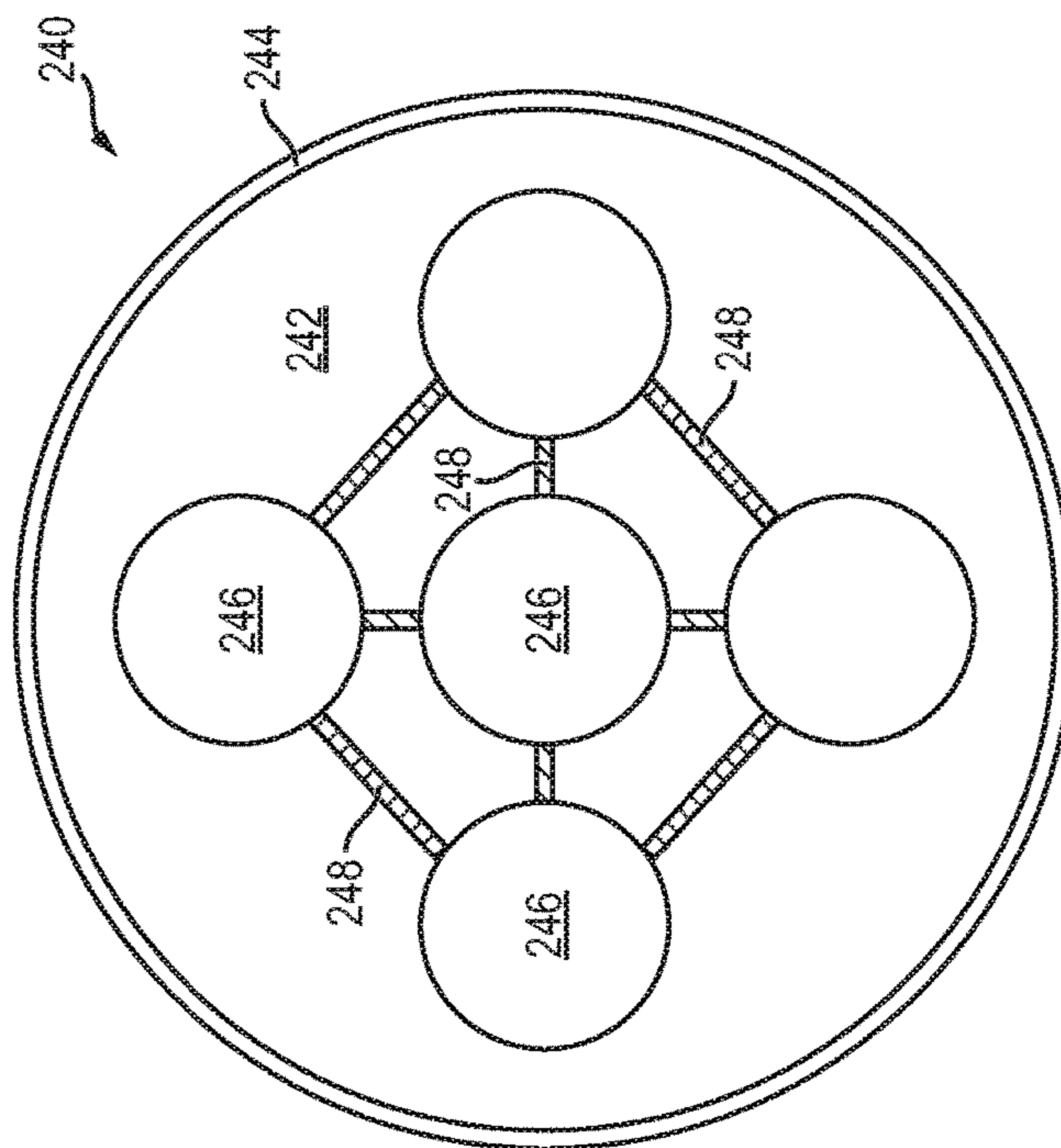


FIG. 4a

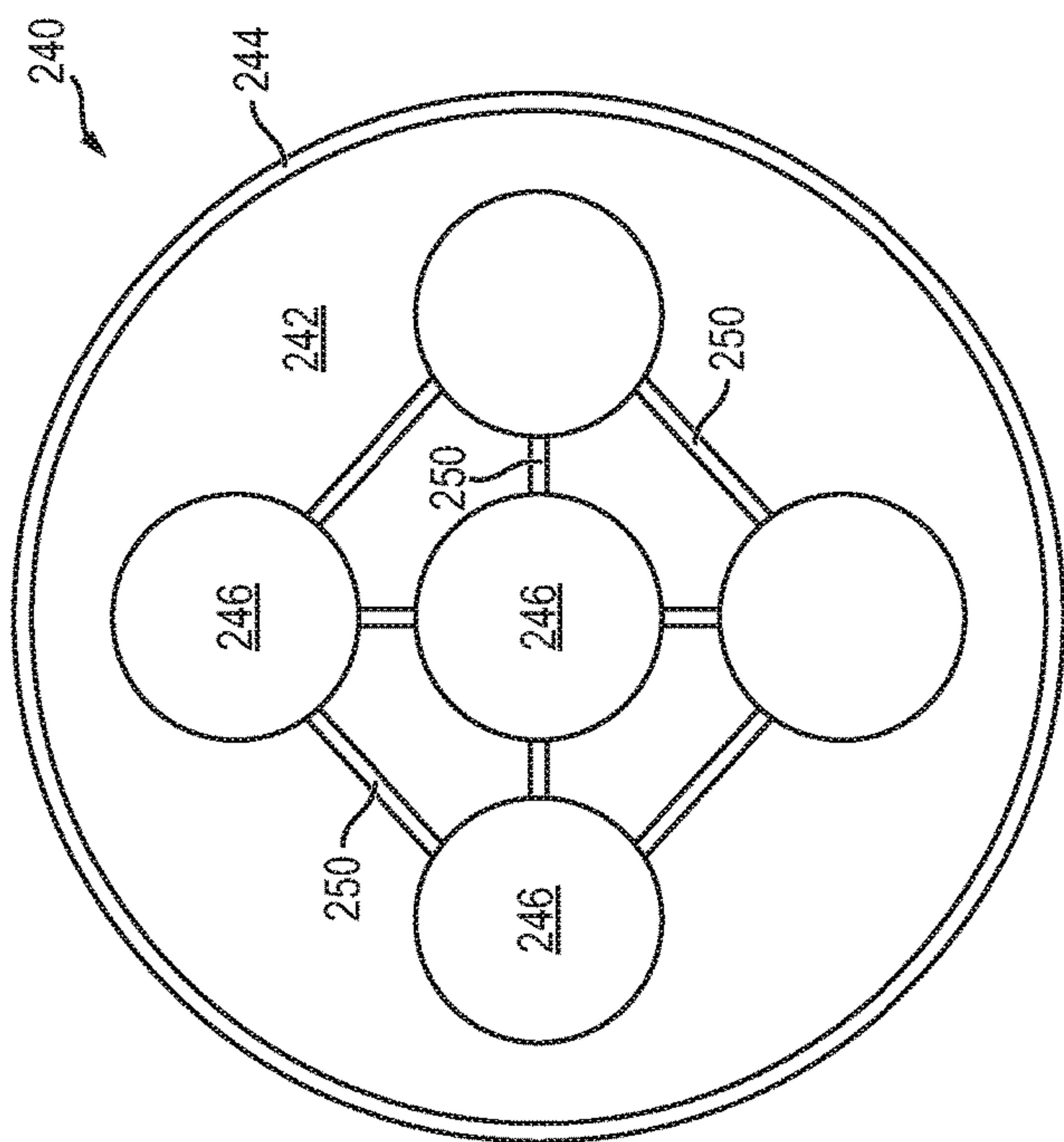


FIG. 4b

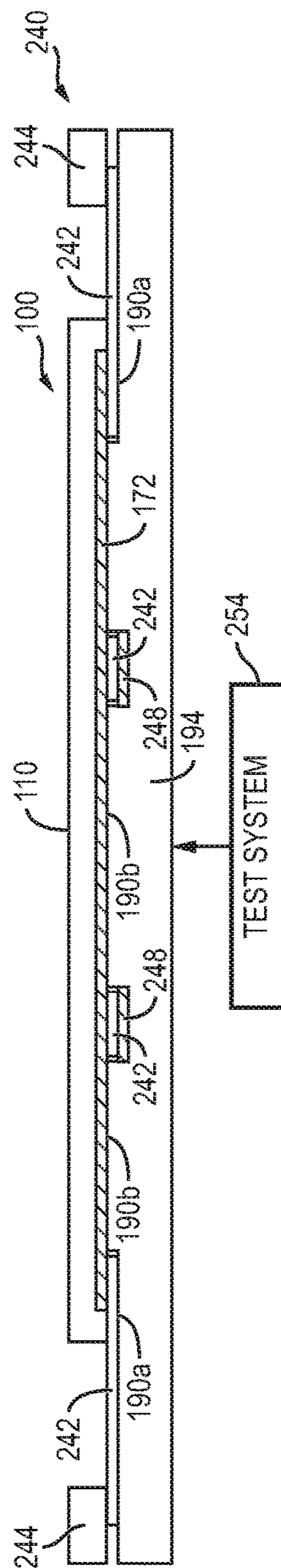


FIG. 4c

SEMICONDUCTOR WAFER AND METHOD OF PROBE TESTING

CLAIM TO DOMESTIC PRIORITY

The present application is a continuation-in-part of U.S. patent application Ser. No. 15/704,246, filed Sep. 14, 2017, which is a continuation of U.S. patent application Ser. No. 15/230,875, now U.S. Pat. No. 9,793,186, filed Aug. 8, 2016, which applications are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor wafer and method of probe testing.

BACKGROUND

Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Semiconductor devices perform a wide range of functions such as analog and digital signal processing, sensors, transmitting and receiving electromagnetic signals, controlling electronic devices, power management, and audio/video signal processing. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, diodes, rectifiers, thyristors, and power metal-oxide-semiconductor field-effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, application specific integrated circuits (ASIC), power conversion, standard logic, amplifiers, clock management, memory, interface circuits, and other signal processing circuits.

A semiconductor wafer includes a base substrate material and plurality of semiconductor die formed on an active surface of the wafer separated by a saw street. Many applications require the semiconductor die to be reduced in height or thickness to minimize the size of the semiconductor package. Testing and inspection of the semiconductor wafer is important for quality assurance and reliability. Testing typically involves contacting a surface of the semiconductor wafer with a test probe. Yet, for large thin semiconductor wafers, wafer test probing often leads to breakage or damage from probe pressure on the thin wafer surface, as well as wafer handling and wafer warpage. The thin semiconductor wafers are subject to warpage. A warped thin semiconductor wafer is difficult to test because the test probes may not make contact with the warped surface.

In some cases, wafer test probing is performed prior to wafer thinning because the large thin wafers, e.g., wafers with a diameter of 150-300 millimeters (mm), may be warped beyond the test probe contact tolerance, or because the thin wafer surface cannot handle the invasive nature of the test. Wafer testing prior to wafer thinning is incomplete because certain features that are added post-wafer thinning, e.g., back-side metal, are not present for the test. In addition, for MOSFETS or wafers with through silicon vias, the current flows through the silicon and out the backside of the thinned wafer, i.e., through the back metal. Testing such devices is impractical for full-thickness wafers. The thickness of the wafers also affects the electrical performance. A thicker T-MOSFET wafer has more resistance than a thin wafer since the current must pass through more silicon. Wafer testing and inspection before all features are present reduces quality assurance, and adds manufacturing cost because an untested die must be assembled before functionality can be confirmed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a*-**1***b* illustrate a semiconductor wafer with a plurality of semiconductor die separated by a saw street;

FIGS. **2***a*-**2***h* illustrate a process of thinning a semiconductor wafer with an edge support ring;

FIGS. **3***a*-**3***s* illustrate a process of probe testing from a backside of the thinned semiconductor wafer through one or more openings in a tape portion of a film frame; and

FIGS. **4***a*-**4***c* illustrate a process of forming conductive channels on the tape.

DETAILED DESCRIPTION OF THE DRAWINGS

The following describes one or more embodiments with reference to the figures, in which like numerals represent the same or similar elements. While the figures are described in terms of the best mode for achieving certain objectives, the description is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the disclosure. The term "semiconductor die" as used herein refers to both the singular and plural form of the words, and accordingly, can refer to both a single semiconductor device and multiple semiconductor devices.

FIG. **1***a* shows semiconductor wafer **100** with a base substrate material **102**, such as silicon, germanium, aluminum phosphide, aluminum arsenide, gallium arsenide, gallium nitride, indium phosphide, silicon carbide, or other bulk semiconductor material. A plurality of semiconductor die **104** is formed on wafer **100** separated by saw street **106**, as described above. Saw street **106** provides singulation areas to separate semiconductor wafer **100** into individual semiconductor die **104**. In one embodiment, semiconductor wafer **100** has a width or diameter of 100-450 mm and thickness of 675-775 micrometers (μm). In another embodiment, semiconductor wafer **100** has a width or diameter of 150-300 mm.

FIG. **1***b* shows a cross-sectional view of a portion of semiconductor wafer **100**. Each semiconductor die **104** has a non-active back surface **108** and an active surface or region **110** containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface or region **110** to implement analog circuits or digital circuits, such as a digital signal processor (DSP), microcontroller, ASIC, power conversion, standard logic, amplifier, clock management, memory, interface circuit, and other signal processing circuit. Semiconductor die **104** may also contain an integrated passive device (IPD), such as inductors, capacitors, and resistors, for RF signal processing. Active surface **110** may contain an image sensor area implemented as semiconductor charge-coupled devices (CCD) and active pixel sensors in complementary metal-oxide-semiconductor (CMOS) or N-type metal-oxide-semiconductor (NMOS) technologies. Alternatively, semiconductor die **104** can be an optical lens, detector, vertical cavity surface emitting laser (VCSEL), waveguide, stacked die, electromagnetic (EM) filter, or multi-chip module.

An electrically conductive layer **112** is formed over active surface **110** using PVD, CVD, electrolytic plating, electroless plating process, evaporation, or other suitable metal deposition process. Conductive layer **112** includes one or more layers of aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), silver (Ag), titanium (Ti), titanium tungsten (TiW), or other suitable electrically conductive material. Conductive layer **112** operates as interconnect pads electrically connected to the circuits on active surface **110**.

In other embodiments, semiconductor wafer **100** represents stacked semiconductor wafers, stacked semiconductor die on the wafer, silicon-on-insulator type wafers, stacked memory wafers, memory devices stacked on a ASIC wafer, stacked through silicon conductive vias (TSV) semiconductor wafers, or any other configuration of stacked wafers, stacked die on wafers, and stacked devices.

FIGS. **2***a*-**2***h* illustrate a process of thinning a semiconductor wafer with an edge support ring. FIG. **2***a* shows an entire area of semiconductor wafer **100** with back surface **108** and active surface **110**. Semiconductor die **104** are present in active surface **110**, see FIGS. **1***a*-**1***b*, but not labeled for purposes of the present explanation. Semiconductor wafer **100** has a pre-grinding thickness T_1 of 675-775 μm.

In FIG. **2***b*, semiconductor wafer **100** is inverted and mounted with active surface **110** oriented to backgrinding tape **120**. In FIG. **2***c*, the entire back surface **108** undergoes a first backgrinding operation with grinder or grinding wheel **122** to remove a portion of base substrate material **102** down to surface **124**. Semiconductor wafer **100** has a post-grinding thickness T_2 of 355 μm between active surface **110** and surface **124**.

In FIG. **2***d*, a second grinding operation is applied to surface **124** using grinder or grinding wheel **128**. Grinding wheel **128** moves in a cyclic, rotating pattern across an interior region or wafer grinding area **130** of semiconductor wafer **100** to remove a portion of base substrate material **102** down to surface **134**. Grinding wheel **128** is controlled to leave edge support ring **136** of base substrate material **102** around a perimeter of semiconductor wafer **100** for structural support. In one embodiment, the post-grinding thickness T_3 of semiconductor wafer **100** is 75 μm or less. In another embodiment, the post-grinding thickness T_3 of semiconductor wafer **100** is 10-50 μm.

FIG. **2***e* shows a top view of grinding wheel **128** removing a portion of surface **134** of semiconductor wafer **100** to reduce the thickness of the semiconductor wafer, and correspondingly semiconductor die **104**, in grinding area **130**, while leaving edge support ring **136** of base substrate material **102** around a perimeter of the semiconductor wafer. Edge support ring **136** has a width W_{136} of 3.0 mm±0.3 mm from inner wall **154** to outer edge **156** around semiconductor wafer **100**. The height of edge support ring **136** is the first post-grinding thickness T_2, which is greater than the second post-grinding thickness T_3 of semiconductor wafer **100**, to maintain structural integrity of the thinner semiconductor wafer.

In FIG. **2***f*, a post-grinding stress relief etch is used to remove or reduce the damage in surface **134** of base substrate material **102** caused by the grinding process. Surface **134** of semiconductor wafer **100** is cleaned with a rinsing solution. An electrically conductive layer **172** is formed over surface **134** using PVD, CVD, electrolytic plating, electroless plating process, evaporation, or other suitable metal deposition process. Conductive layer **172** includes one or more layers of Al, Cu, Sn, Ni, Au, Ag, Ti, TiW, or other suitable electrically conductive material. Conductive layer **172** provides back-side electrical interconnect for semiconductor die **104**. Conductive layer **172** makes connection to the circuits on active surface **110** through TSV. Conductive layer **172** is patterned into electrically common or electrically isolated portions according to the function of semiconductor die **104**. Backgrinding tape **120** is removed by exposing the tape to ultraviolet (UV) light and peeling off.

In FIG. **2***g*, the thinned semiconductor wafer **100** is mounted with active surface **110** oriented to tape portion **176** of film frame or carrier **178**. In FIG. **2***h*, edge support ring **136** is removed to be planar with or just above (10-13 μm) conductive layer **172** or surface **134**.

FIGS. **3***a*-**3***s* illustrate various configurations for probe testing the semiconductor wafer. In FIG. **3***a*, the thinned semiconductor wafer **100** is removed from film frame **178** and positioned above film frame or carrier **180** with conductive layer **172** on surface **134** oriented toward the film frame. Semiconductor die **104** on the thinned semiconductor wafer **100** have a full feature set, i.e., all functional components and layers have been formed, ready for probe testing of the final semiconductor die. Film frame **180** includes tape portion **182** and edge support **184**. In particular, tape portion **182** includes an opening **186** extending through a center region of the tape portion. The thinned semiconductor wafer **100** is positioned over film frame **180** with conductive layer **172** aligned and centered with opening **186**. FIG. **3***b* shows a top view of film frame **180** with tape portion **182** and opening **186** extending through a center region of the tape portion. Semiconductor wafer **100** is mounted to tape portion **182** of film frame **180** with a portion of conductive layer **172** disposed over opening **186**. FIG. **3***c* shows a top view of semiconductor wafer **100** mounted to tape portion **182** of film frame **180**. Conductive layer **172** is accessible through opening **186** in tape portion **182**.

In FIG. **3***d*, semiconductor wafer **100** and film frame **180** are positioned over surface **190** of wafer probing chuck **194**. Surface **190** has lower portion **190***a* and raised portion **190***b*. The raised portion **190***b* is aligned with opening **186**. FIG. **3***e* shows film frame **180** with semiconductor wafer **100** mounted to surface **190** of wafer probing chuck **194** with tape portion **182** contacting lower portion **190***a* of surface **190**, and raised portion **190***b* extending through opening **186** to contact conductive layer **172**. In one embodiment, wafer probing chuck **194** draws a vacuum through ports **193** to hold tape portion **182** and semiconductor wafer **100** securely in place with surface **134** and a first portion of conductive layer **172** held flat against and in contact with tape portion **182**, tape portion **182** held flat against and in contact with lower portion **190***a* of surface **190**, and a second portion of conductive layer **172** held flat against and in contact with raised portion **190***b* of surface **190**. In FIG. **3***f*, a porous ceramic chuck **194**, with the same surface **190** including lower portion **190***a* and raised portion **190***b*, evenly distributes the vacuum forces to hold semiconductor wafer **100** and film frame **180** flat against lower portion **190***a* and raised portion **190***b* of surface **190**. Semiconductor wafer **100** and film frame **180** being held flat against lower portion **190***a* and raised portion **190***b* of surface **190** by vacuum ports **193** or porous chuck **194** keeps the wafer stable and planar during probe testing. Alternatively, tape portion **182** and semiconductor wafer **100** are held securely in place by a press-fit with force F, as shown in FIG. **3***g*, with surface **134** and a first portion of conductive layer **172** held flat against and in contact with tape portion **182**, tape portion **182** held flat against and in contact with lower portion **190***a* of surface **190** of chuck **195**, and a second portion of conductive layer **172** held flat against and in contact with raised portion **190***b*

of surface **190**. Chuck **195** has the same surface **190** with lower portion **190***a* and raised portion **190***b*.

Semiconductor wafer **100** undergoes electrical testing and inspection as part of a quality control process. Manual visual inspection and automated optical systems are used to perform inspections on semiconductor wafer **100**. Software can be used in the automated optical analysis of semiconductor wafer **100**. Visual inspection methods may employ equipment such as a scanning electron microscope, high-intensity or ultra-violet light, metallurgical microscope, or optical microscope. Semiconductor wafer **100** is inspected for structural characteristics including warpage, thickness variation, surface particulates, irregularities, cracks, delamination, contamination, and discoloration.

The active and passive components within semiconductor die **104** undergo testing at the wafer-level for electrical performance and circuit function. Each semiconductor die **104** is tested for functionality and electrical parameters. The raised portion **190***b* of surface **190** of wafer probing chuck **194** makes electrical contact with conductive layer **172** through opening **186**. A computer controlled test system **196** sends electrical test signals through wafer probing chuck **194** and raised portion **190***b* of surface **190**, which extends through opening **186**, to provide electrical stimuli to conductive layer **172**. Alternatively, computer controlled test system **196** sends electrical test signals through conductive channels within wafer probing chuck **194** and raised portion **190***b* of surface **190** to provide electrical stimuli to conductive layer **172**. Conductive layer **172** is coupled to circuits on active surface **110** through TSV or vertically formed semiconductor devices. Semiconductor die **104** responds to the electrical stimuli, which is measured by computer test system **196** and compared to an expected response to test functionality of the semiconductor die.

The testing of semiconductor wafer **100** from the backside directly to conductive layer **172** is achieved through raised portion **190***b* of surface **190** of wafer probing chuck **194** extending through opening **186** in tape portion **182** of film frame **180**. Many testing procedures can be accomplished with wafer probe contact of raised portion **190***b* to conductive layer **172**. For example, the electrical tests may include circuit functionality, lead integrity, resistivity, continuity, reliability, junction depth, ESD, RF performance, drive current, threshold current, leakage current, and operational parameters specific to the component type. The testing is conducted with the thinned semiconductor wafer **100** after wafer grinding. The thinned semiconductor wafer **100** remains flat and stable by nature of lower portion **190***a* and raised portion **190***b* of surface **190** of wafer probing chuck **194** held against conductive layer **172**. The inspection and electrical testing of semiconductor wafer **100**, after wafer thinning, enables semiconductor die **104**, with a complete feature set that passes, to be designated as known good die for use in a semiconductor package.

Wafer level testing also encompasses advanced testing procedures, including curve tracing of semiconductor wafer **100** or other characterization of the device, to evaluate detailed electrical and thermal performance of the thin wafer or stacked wafer.

Semiconductor wafer **100** can also be tested from active surface **110**, as shown in FIG. **3***h*. Each semiconductor die **104** is tested for functionality and electrical parameters using a test probe head **200** including a plurality of probes or test leads **202**, or other testing device. Probes **202** are used to make electrical contact with nodes or conductive layer **112** on each semiconductor die **104** and provide electrical stimuli to interconnect pads **112**. Semiconductor die **104** responds to the electrical stimuli, which is measured by computer test system **206** and compared to an expected response to test functionality of the semiconductor die. The electrical tests may include circuit functionality, lead integrity, resistivity, continuity, reliability, junction depth, ESD, RF performance, drive current, threshold current, leakage current, and operational parameters specific to the component type. The inspection and electrical testing of semiconductor wafer **100** enables semiconductor die **104** that pass to be designated as known good die for use in a semiconductor package.

The tape portion may have multiple openings to provide access to different areas of conductive layer **172**. As noted above, conductive layer **172** is patterned into electrically common or electrically isolated portions according to the function of semiconductor die **104**. FIG. **3***i* shows a top view of film frame **210** including tape portion **212**, edge support **214**, and multiple openings **216**. Tape portion **212** has as many openings **216** as necessary to perform testing of requisite areas of conductive layer **172**. Openings **216** can be cut or punched through tape portion **212** prior to mounting the tape portion to edge support **214**, or after mounting the tape portion to the edge support. Cutting openings **216** prior to mounting tape portion **212** to edge support **214** allows for standard cut-out patterns to match specific wafers **100**, e.g., a perforated tape. Cutting openings **216** after mounting tape portion **212** to edge support **214** allows for a cut-out pattern customized for a specific wafer **100**. Openings **216** can be cut using a laser or blade, or simply remove pre-cut portions of the tape.

Semiconductor wafer **100** is then mounted to tape portion **212**, as shown in FIG. **3***j*. In this case, wafer probing chuck **194** would have multiple raised portions **190***b* aligned with openings **216**. Film frame **210** with semiconductor wafer **100** is mounted to surface **190** of wafer probing chuck **194** with tape portion **212** contacting lower portion **190***a* of surface **190** and multiple raised portion **190***b* extending through multiple openings **216** to contact different areas of conductive layer **172**. Tape portion **212** and semiconductor wafer **100** are held securely in place by a press-fit or vacuum assist with surface **134** and first portions of conductive layer **172** held flat against and in contact with tape portion **212**, tape portion **212** held flat against and in contact with lower portion **190***a* of surface **190**, and second portions of conductive layer **172** held flat against and in contact with raised portion **190***b* of surface **190**. Semiconductor wafer **100** and film frame **210** being held flat against lower portions **190***a* and raised portions **190***b* of surface **190** by press-fit or vacuum assist keeps the wafer stable and planar during probe testing.

The multiple raised portions **190***b* of surface **190** of wafer probing chuck **194** make electrical contact with corresponding areas of conductive layer **172** through openings **216**. A computer controlled test system **220** sends electrical test signals through wafer probing chuck **194** and raised portions **190***b* of surface **190**, which extends through openings **216**, to provide electrical stimuli to different areas of conductive layer **172**. Semiconductor die **104** responds to the electrical stimuli, which is measured by computer test system **220** and compared to an expected response to test functionality of the semiconductor die.

In one embodiment, as shown in FIG. **3***k*, semiconductor wafer **100** is tested from active surface **110**, see FIG. **3***h*, with electrical connection from ground reference node **221** to conductive layer **172** being made through openings **216** in tape portion **212**. Multiple portions of conductive layer **172** can be electrically connected to external ground reference

node **221** through openings **216**. A sample portion of semiconductor wafer **100** can be tested from active surface **110**.

Alternatively, wafer ring holder **222** with grip ring **224**, as shown in FIG. **3***l*, can be used for mounting semiconductor wafer **100**. Wafer ring holder **222** is typically plastic or other light-weight material for low-cost and ease of handling. Grip ring **224** secures and holds tape portion **225** for mounting semiconductor wafer **100**. Openings **226** can be formed in tape portion **225**, as described above. Other tape holders can be used to secure tape portion **225** when mounting semiconductor wafer **100**.

FIG. **3***m* shows semiconductor wafer **100** mounted to tape portion **225** on wafer ring holder **222** with conductive layer **172** oriented toward the tape portion and active surface **110** oriented away from the tape portion. FIG. **3***n* shows semiconductor wafer **100** mounted to tape portion **225** on wafer ring holder **222** with active surface **110** oriented toward the tape portion and conductive layer **172** oriented away from the tape portion. With the use of TSV, the orientation of semiconductor wafer **100** is interchangeable. Semiconductor wafer **100** can have bumps **227** on active surface **110**, as shown in FIG. **3***o*, or no bumps, as in FIG. **3***k*. Semiconductor wafer **100** can be tested with active surface **110** and bumps **227** oriented toward tape portion **225** or away from the tape portion. Semiconductor wafer **100** can be tested with active surface **110** and no bumps oriented toward tape portion **225** or away from the tape portion. A sample portion of semiconductor wafer **100** can be tested with active surface **110** of semiconductor wafer **100** oriented toward tape portion **225** or away from the tape portion.

In another embodiment, semiconductor wafer **100** is mounted to tape portion **225** without openings **226** to avoid stretching, non-uniformity, or other distortion in the tape portion or openings, see FIG. **3***p*. Tape portion **225** without openings **226** can also be placed over semiconductor wafer **100**. Multiple semiconductor wafers **100** can be mounted to tape sheet or roll while maintaining uniform tension across the tape sheet. Once semiconductor wafer **100** is mounted, openings **226** are cut through tape portion **225** using a laser, blade, or by simply removing pre-cut portions of the tape, similar to FIG. **3***l*. Tape portion **225** with semiconductor wafer **100** is affixed to grip ring **224** of wafer ring holder **222** either prior to or after cutting openings **226**.

FIG. **3***q* shows conductive traces **228** formed on a surface of tape portion **225** as mounted to wafer ring holder **222** with precise placement of the conductive paths. Tape portion **225** can be laminated to wafer ring holder **222** for access orientation and alignment of conductive traces **228**, which are then formed by lamination, printing, or shadow mask metal film deposition. In FIG. **3***r*, semiconductor wafer **100** is mounted to tape portion **225** and aligned with conductive traces **228** formed on tape portion **225** to make electrical contact and perform the necessary probe testing. In this case, test probes **230** contact conductive traces **228** from the topside, outside wafer ring holder **222**. Test probe signals are routed from test probes **230** along conductive traces **228** to conductive layer **172** in order to test functionality and electrical parameters of semiconductor wafer **100**. FIG. **3***s* shows semiconductor wafer **100** mounted with bumps **227** to tape portion **225** and aligned with conductive traces **228** formed on tape portion **225** to make electrical contact and perform the necessary probe testing. In this case, test probes **230** contact conductive traces **228** from the topside, outside wafer ring holder **222**. Test probe signals are routed from test probes **230** along conductive traces **228** to bumps **227** in order to test functionality and electrical parameters of semiconductor wafer **100**.

In another embodiment, similar to FIGS. **3***i*-**3***j*, the film frame or wafer ring holder may have multiple openings and conductive traces or channels formed in the tape portion of the wafer ring holder to provide access to different areas of the conductive layer. FIG. **4***a* shows a top view of wafer ring holder **240** including tape portion **242**, grip ring **244**, and multiple openings **246**. Conductive traces **248** formed on the surface of tape portion **242** or formed through the tape portion. Alternatively, tape portion **242** may be made with channels of conductive carbon **240**, as shown in FIG. **4***b*. Tape portion **242** has as many multiple openings **246** and conductive traces **248** or channels **250** as necessary to perform probe testing of requisite areas of conductive layer **172**. In another embodiment, any portion or the entire tape portion **242** may be conductive to perform testing of requisite areas of conductive layer **172**. Tape portion **242** and semiconductor wafer **100** are held securely in place by a press-fit or vacuum assist with surface **134** and first portions of conductive layer **172** held flat against and in contact with tape portion **242**, tape portion **242** held flat against and in contact with lower portion **190***a* of surface **190**, and second portions of conductive layer **172** held flat against and in contact with raised portion **190***b* of surface **190**. Semiconductor wafer **100** and wafer ring holder **240** being held flat against lower portions **190***a* and raised portions **190***b* of surface **190** by press-fit or vacuum assist keeps the wafer stable and planar during probe testing.

In FIG. **4***c*, the multiple raised portions **190***b* of surface **190** of wafer probing chuck **194** make electrical contact with corresponding areas of conductive layer **172** through openings **246** and conductive traces **248** or channels **250**. Computer controlled test system **254** sends electrical test signals through wafer probing chuck **194** and raised portions **190***b* of surface **190**, which extends through openings **246**, to provide electrical stimuli through conductive traces **248** or channels **250** to different areas of conductive layer **172**. Semiconductor die **104** responds to the electrical stimuli, which is measured by computer test system **254** and compared to an expected response to test functionality of the semiconductor die.

The wafer ring holder and semiconductor wafer **100** are moved from wafer probing chuck **194** and the thinned semiconductor wafer **100** is singulated through saw streets **106** using a saw blade or laser cutting tool or plasma etch into individual semiconductor die **104**. The individual semiconductor die **104** from the thinned semiconductor wafer **100** have been probe tested in the final configuration of the semiconductor die.

While one or more embodiments have been illustrated and described in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present disclosure.

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor wafer;

providing a wafer holder including a tape portion with an opening through the tape portion;

mounting the semiconductor wafer over the opening in the tape portion of the wafer holder; and

providing an electrical connection to the semiconductor wafer through the opening in the tape portion during probe test.

2. The method of claim **1**, further including forming a plurality of bumps over the semiconductor wafer.

3. The method of claim **1**, wherein providing the semiconductor wafer includes providing a stacked semiconductor wafer.

4. The method of claim **1**, further including forming a conductive trace over the tape portion.

5. The method of claim **1**, further including forming the opening through the tape portion after mounting the tape portion to the wafer holder.

6. The method of claim **1**, further including forming the opening through the tape portion prior to mounting the tape portion to the wafer holder.

7. An apparatus for probe testing a semiconductor device, comprising:

a semiconductor wafer; and

a wafer holder including a tape portion with an opening through the tape portion, wherein the semiconductor wafer is mounted over the opening in the tape portion of the wafer holder with an electrical connection to the semiconductor wafer through the opening in the tape portion during probe test.

8. The apparatus of claim **7**, further including a plurality of bumps formed over the semiconductor wafer.

9. The apparatus of claim **7**, wherein the semiconductor wafer includes a stacked semiconductor wafer.

10. The apparatus of claim **7**, further including a conductive trace formed over the tape portion.

11. The apparatus of claim **7**, wherein an active surface of the semiconductor wafer is oriented toward the tape portion.

12. The apparatus of claim **7**, wherein a non-active surface of the semiconductor wafer is oriented toward the tape portion.

13. The apparatus of claim **7**, wherein the electrical connection to the semiconductor wafer through the opening in the tape portion is a ground reference node.

14. An apparatus for probe testing a semiconductor device, comprising:

a semiconductor wafer; and

a wafer holder including a tape portion; and

a conductive trace formed on the tape portion, wherein the semiconductor wafer is mounted over the tape portion of the wafer holder with an electrical connection to the semiconductor wafer through the conductive trace during probe test.

15. The apparatus of claim **14**, further including a plurality of bumps formed over the semiconductor wafer.

16. The apparatus of claim **14**, wherein the semiconductor wafer includes a stacked semiconductor wafer.

17. The apparatus of claim **14**, wherein an active surface of the semiconductor wafer is oriented toward the tape portion.

18. The apparatus of claim **14**, wherein a non-active surface of the semiconductor wafer is oriented toward the tape portion.

19. The apparatus of claim **14**, further including an opening through the tape portion.

20. The apparatus of claim **14**, further including a conductive layer over a non-active surface of the semiconductor wafer.

* * * * *