(19) **United States**(12) **Patent Application Publication**
Glovinsky(10) **Pub. No.: US 2017/0288546 A1**(43) **Pub. Date: Oct. 5, 2017**(54) **ZERO VOLTAGE SWITCHING**(71) Applicant: **Solaredge Technologies Ltd.**, Herzliya
Pituach (IL)(72) Inventor: **Tzachi Glovinsky**, Petah Tikva (IL)(21) Appl. No.: **15/488,858**(22) Filed: **Apr. 17, 2017****Related U.S. Application Data**

(63) Continuation of application No. 14/585,280, filed on Dec. 30, 2014, now Pat. No. 9,660,527, which is a continuation of application No. 13/338,330, filed on Dec. 28, 2011, now Pat. No. 8,957,645, which is a continuation of application No. 12/409,604, filed on Mar. 24, 2009, now Pat. No. 8,111,052.

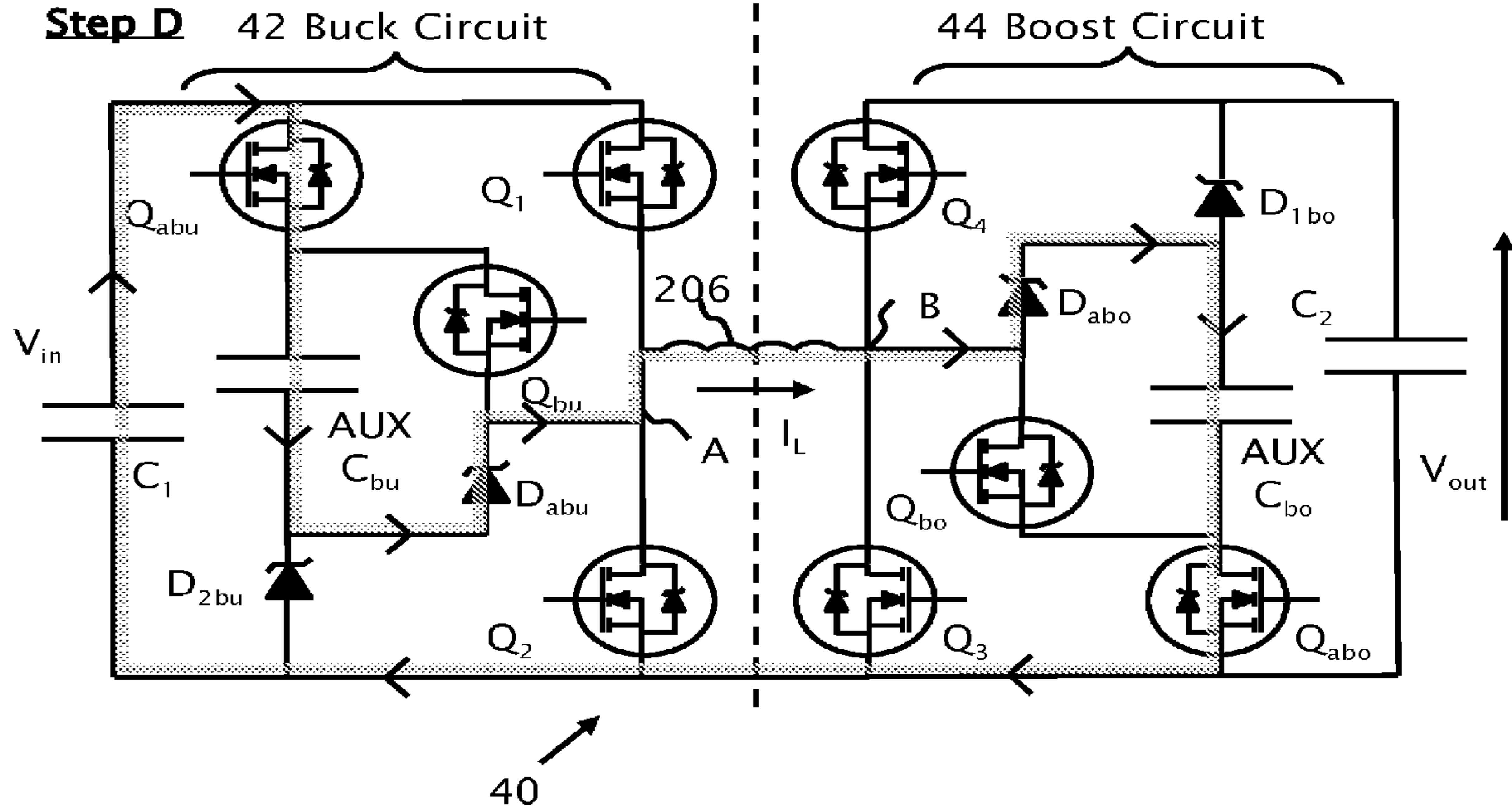
(60) Provisional application No. 61/039,046, filed on Mar. 24, 2008.

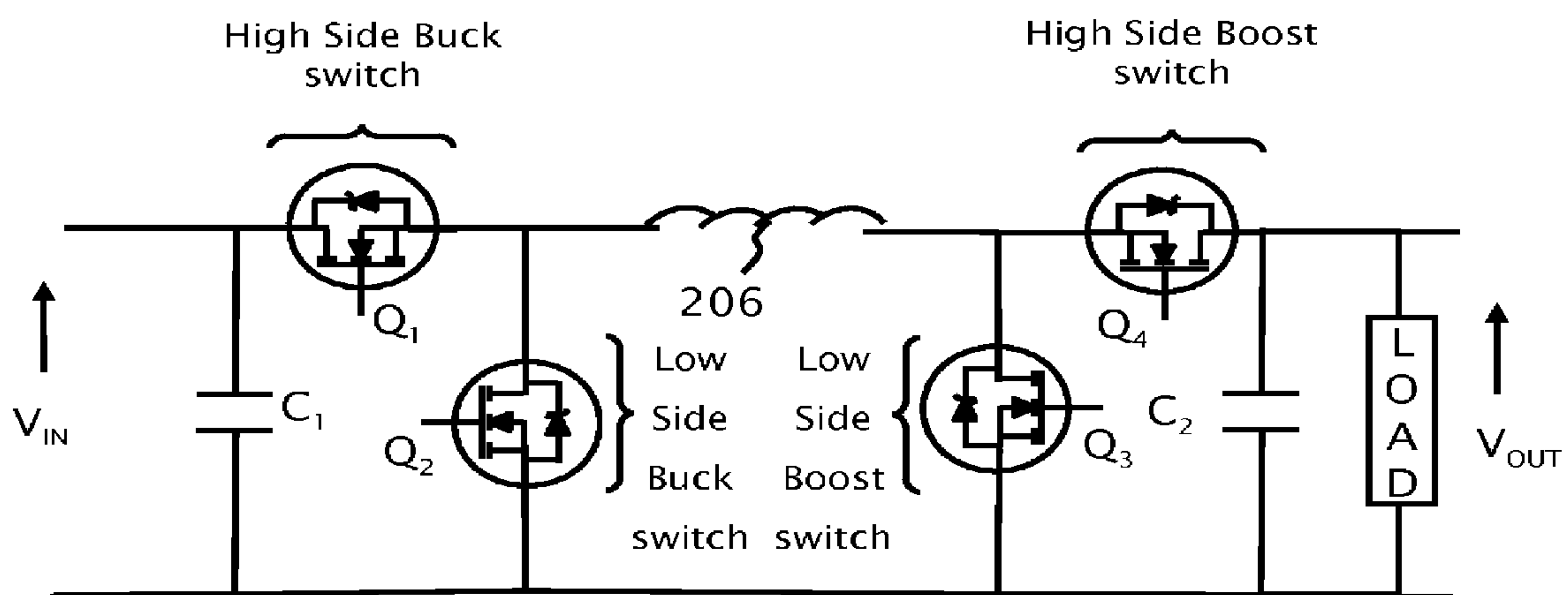
Publication Classification(51) **Int. Cl.***H02M 3/158* (2006.01)*H02M 7/5387* (2006.01)*H02M 1/34* (2006.01)(52) **U.S. Cl.**CPC *H02M 3/158* (2013.01); *H02M 1/34*
(2013.01); *H02M 7/5387* (2013.01); *H02M*
2007/4811 (2013.01)

(57)

ABSTRACT

A method for providing non-resonant zero-voltage switching in a switching power converter. The switching power converter converts power from input power to output power during multiple periodic switching cycles. The switching power converter includes a main switch and an auxiliary capacitor adapted for connecting to the main switch, and an inductor connectible to the auxiliary capacitor. When the main switch is on, a previously charged (or previously discharged) auxiliary capacitor is connected to the main switch with auxiliary switches. The main switch is switched off with zero voltage while discharging non-resonantly (charging) the auxiliary capacitor by providing a current path to the inductor. The auxiliary capacitor is disconnected from the main switch. The voltage of the auxiliary capacitor is charged and discharged alternatively during subsequent switching cycles. The voltage of the auxiliary capacitor stays substantially the same until the subsequent turn off of the main switch during the next switching cycle with substantially no energy loss in the auxiliary capacitor.





20 ↗

Fig. 1 (Conventional art)

Q_1 on, Q_2 off, Q_3 on, Q_4 off (Buck Phase)

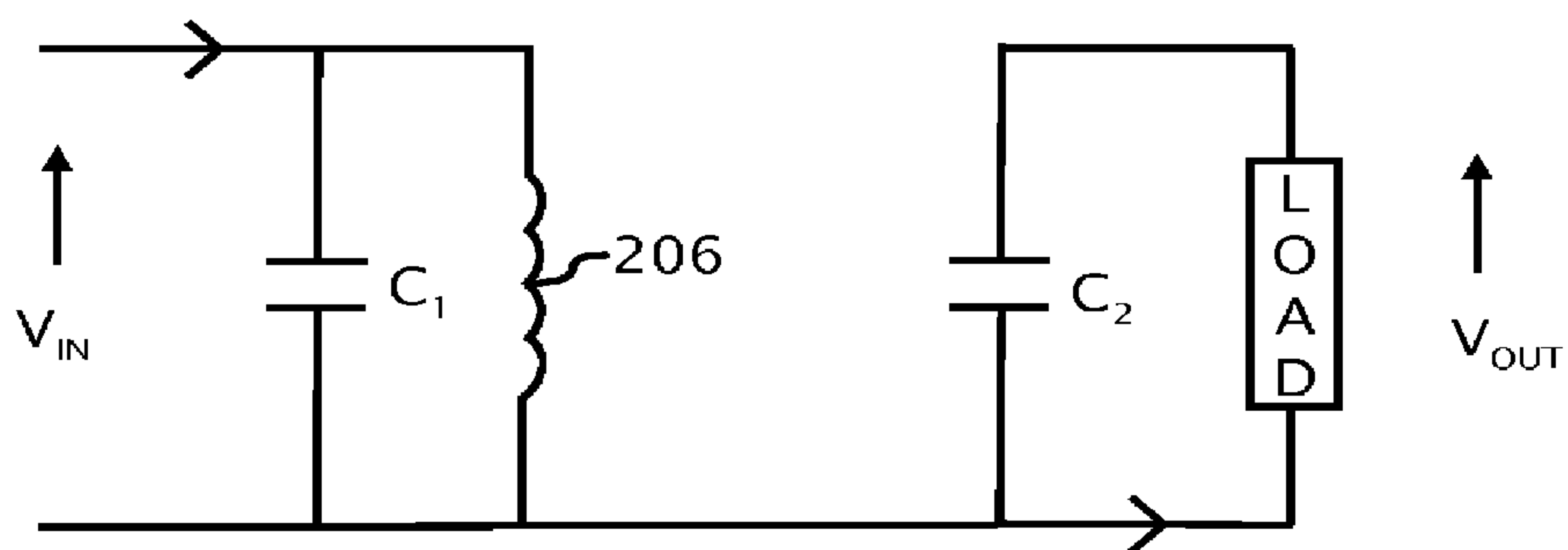


Fig. 2a (Conventional art)

Q_1 off, Q_2 on, Q_3 off, Q_4 on (Boost phase)

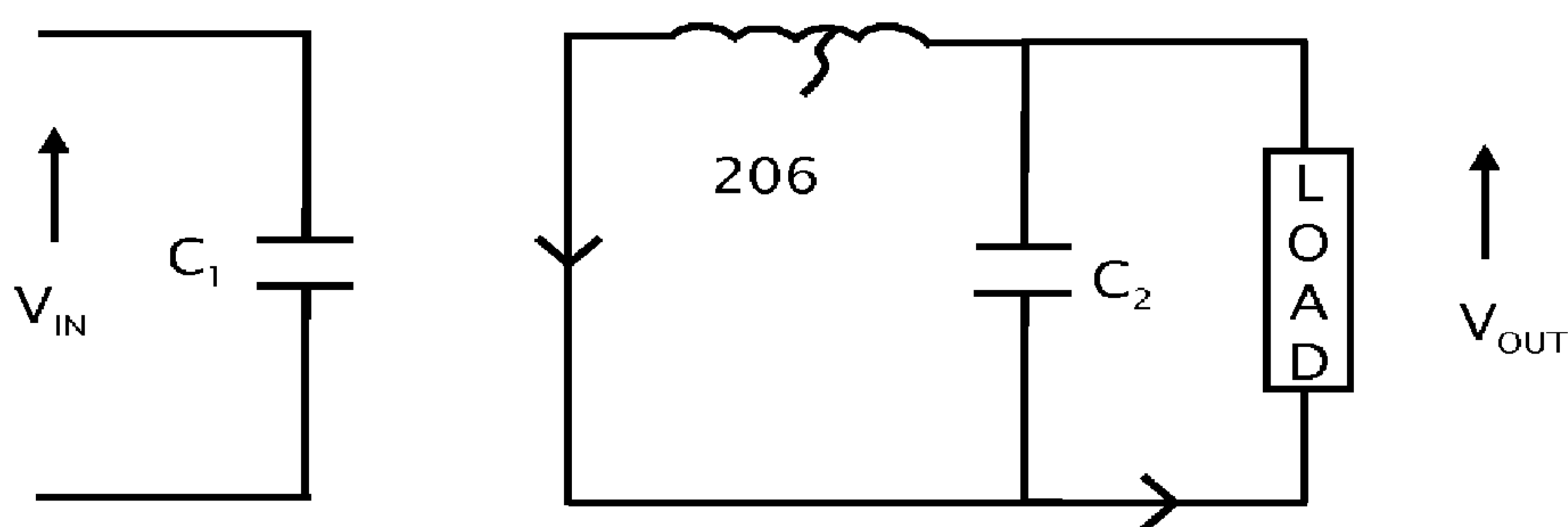


Fig. 2b (Conventional art)

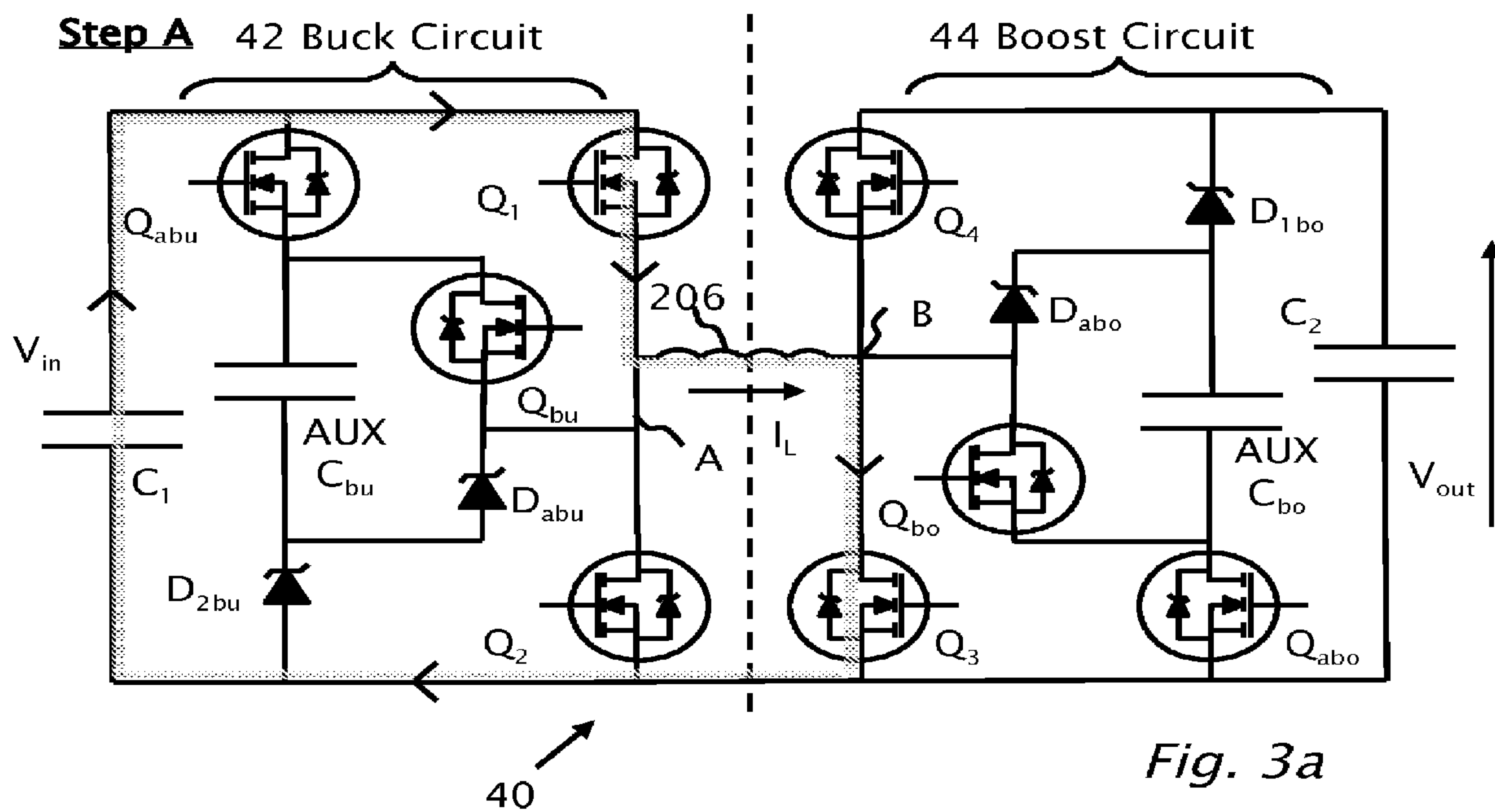
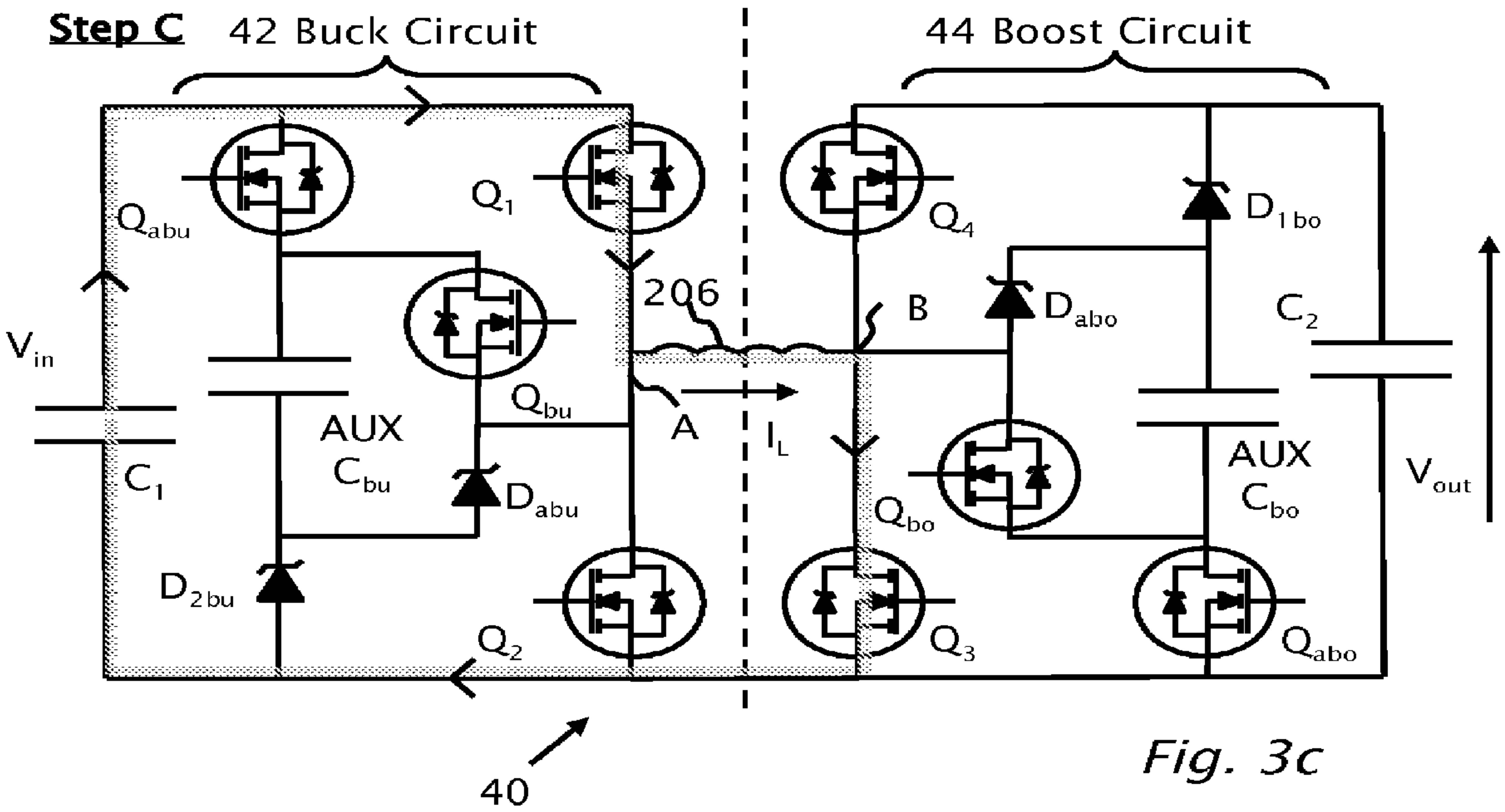
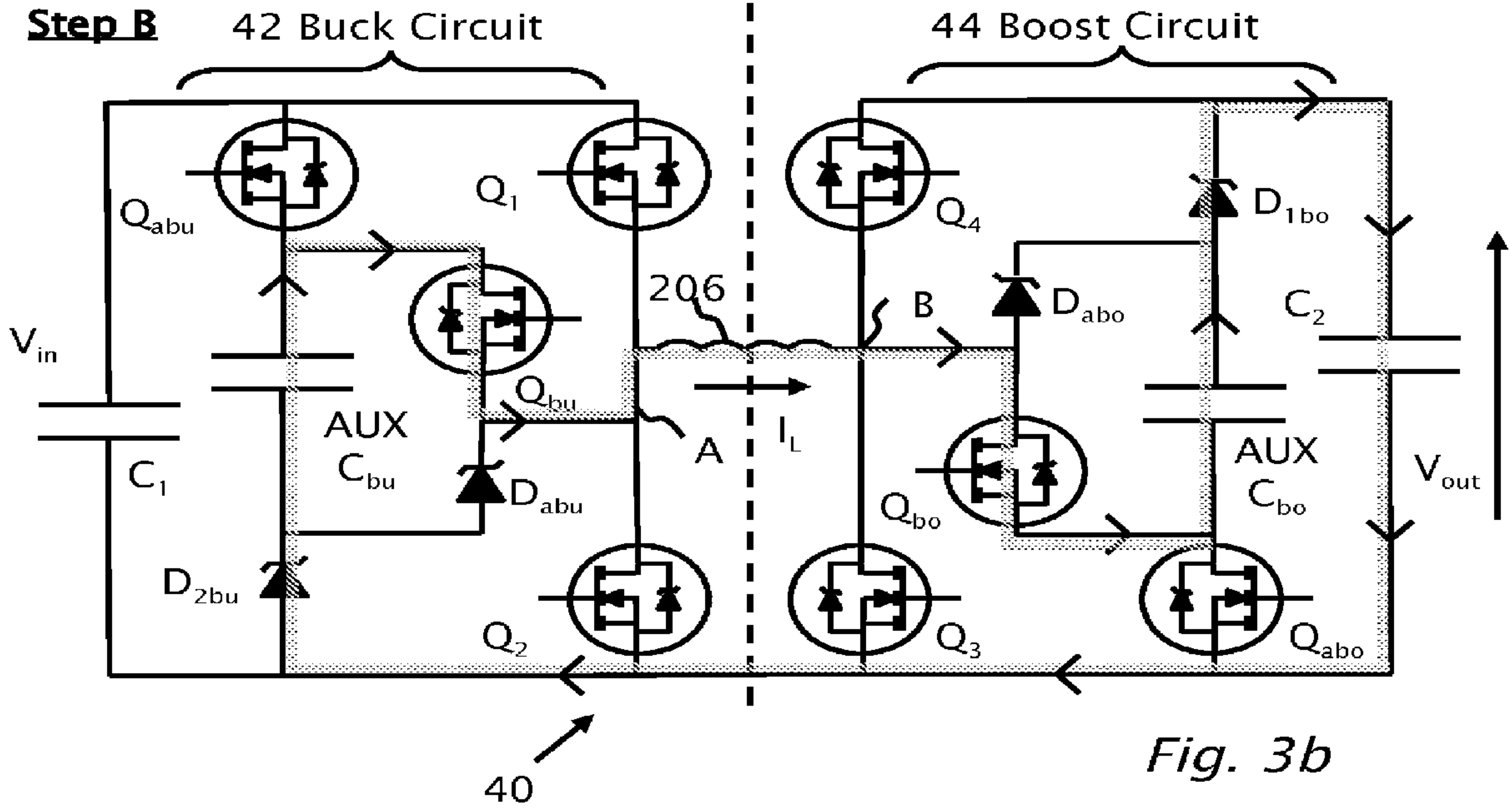
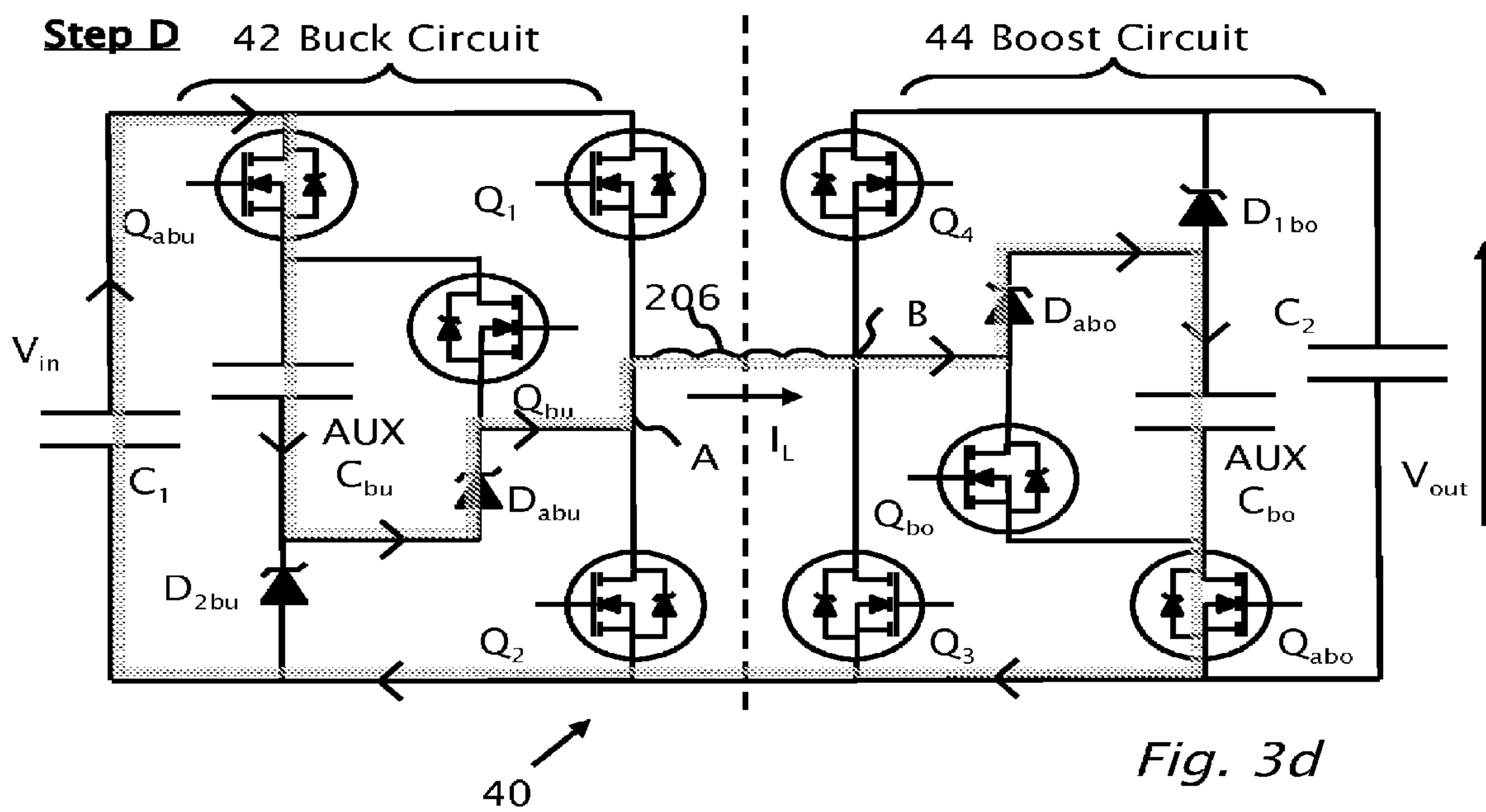
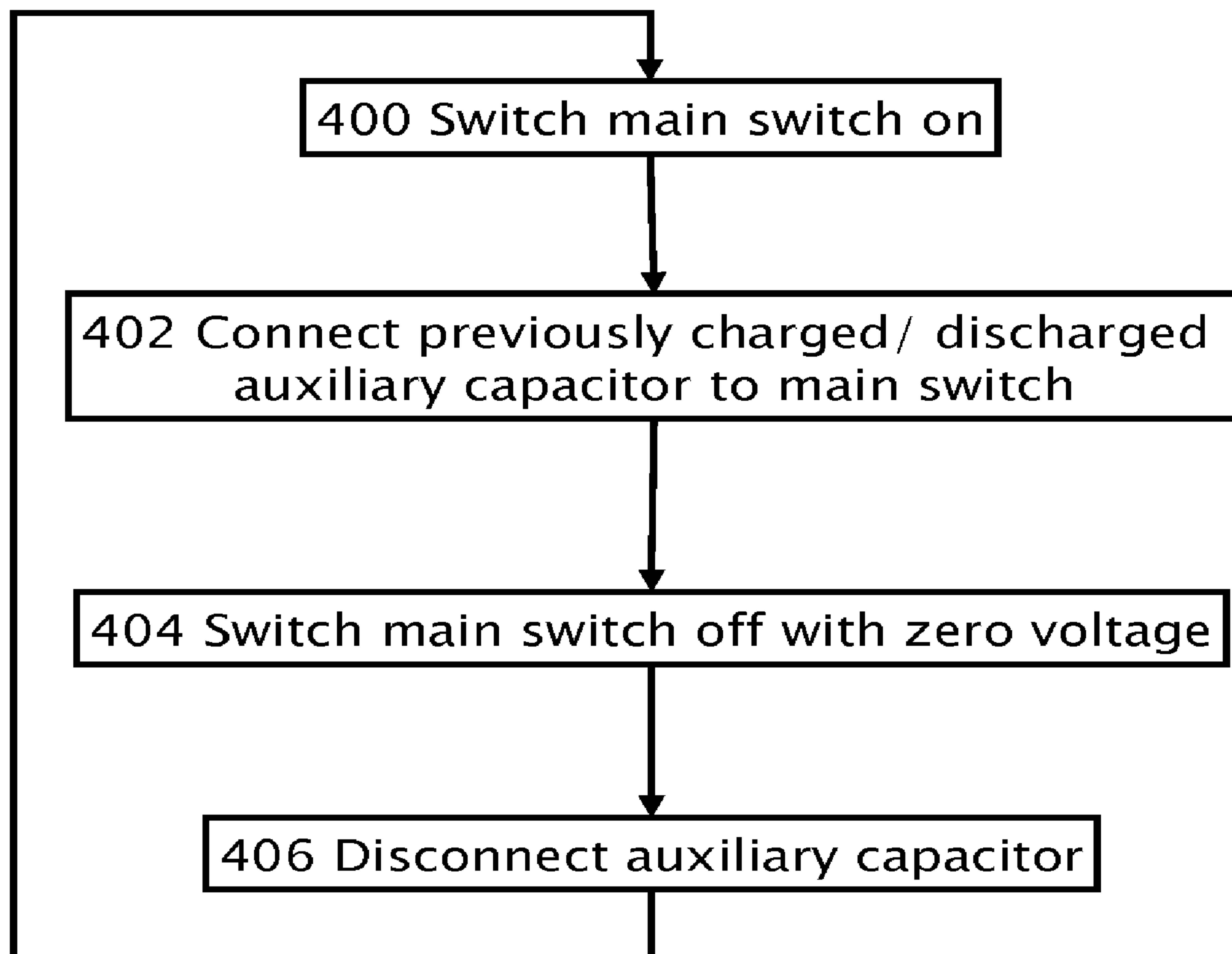
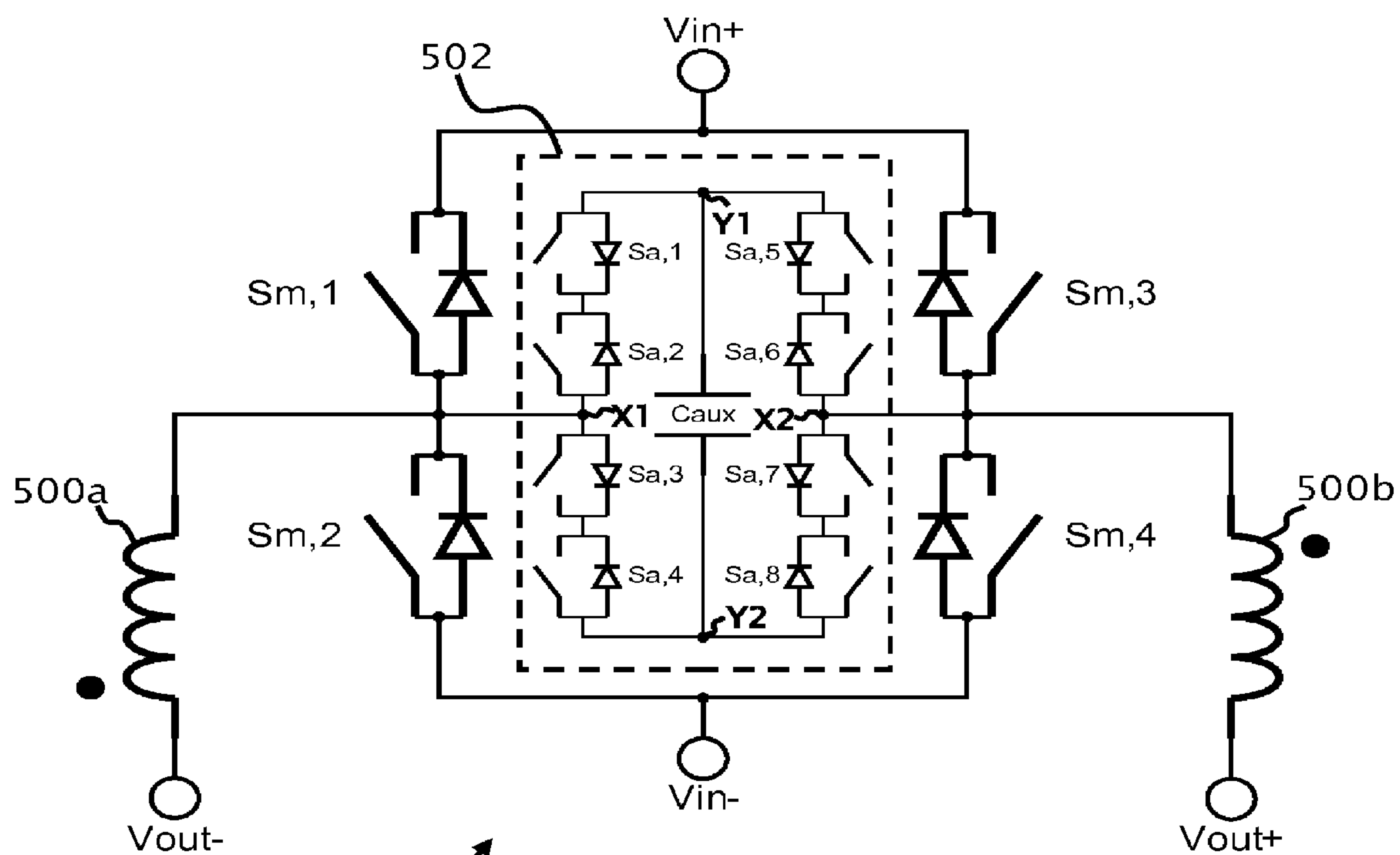


Fig. 3a





*Fig. 4*



50

Fig. 5

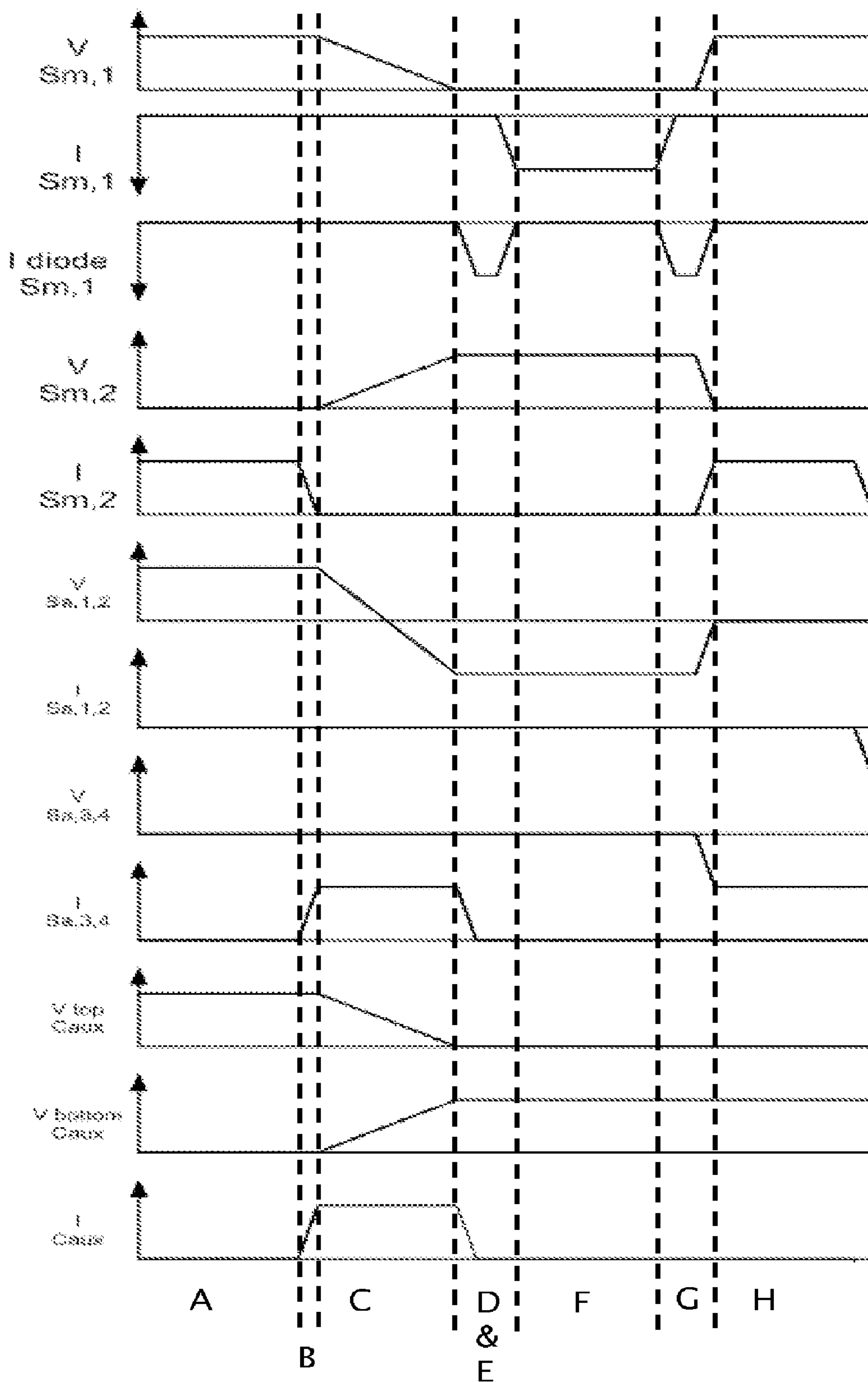


Fig. 6

ZERO VOLTAGE SWITCHING

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation application of pending U.S. patent application Ser. No. 12/409,604 filed on Mar. 24, 2009 by the present inventors.

[0002] The present application claims priority from U.S. provisional application 61/039046 filed on Mar. 24, 2008 by the present inventors.

BACKGROUND

1. Technical Field

[0003] The present invention relates to switching converters and to specifically a method and devices for zero voltage switching for reducing switching losses in switching converters.

2. Description of Related Art

[0004] FIG. 1 shows a typical conventional buck-boost DC-to-DC converter circuit **20**. The buck circuit of buck-boost DC-to-DC converter **20** has an input voltage V_{in} with an input capacitor C_1 connected in parallel across V_{in} . Two switches are implemented as field effect transistors (FET) with integral diodes: a high side buck switch Q_1 and a low side buck switch Q_2 connected in series by connecting the source of Q_1 to the drain of Q_2 . The drain of Q_1 and the source of Q_2 are connected parallel across an input capacitor C_1 . A node A is formed between switches Q_1 and Q_2 to which one end of an inductor **206** is connected. The other end of inductor **206** is connected to the boost circuit of buck-boost DC-to-DC converter **20** at a node B. Node B connects two switches: a high side boost switch Q_4 and a low side boost switch Q_3 together in series where the source of Q_4 connects to the drain of Q_3 to form node B. The drain of Q_4 and the source of Q_3 connect across an output capacitor C_2 to produce the output voltage V_{out} of buck-boost DC-to-DC converter **20**.

[0005] FIG. 2a illustrates the buck phase or on-state circuit of DC-to-DC converter circuit **20** shown in FIG. 1, the input voltage source V_{in} is directly connected to inductor **206** and the load is isolated from V_{in} because Q_1 is on, Q_2 is off, Q_3 is on and Q_4 is off. These switch positions: Q_1 on, Q_2 off, Q_3 on and Q_4 off; result in accumulating energy in inductor **206** since source V_{in} is directly connected to inductor **206**. In the on-state, output capacitor C_2 supplies energy to the load.

[0006] FIG. 2b illustrates the boost phase or off-state circuit of DC-to-DC converter circuit **20**, Inductor **206** is connected in parallel across the load and capacitor C_2 because Q_1 is off, Q_2 is on, Q_3 is off and Q_4 is on. Q_1 being off isolates inductor **206** from the input voltage (V_{in}) and capacitor (C_1). The stored energy in inductor **206** (as a result of the previous On-state) is transferred from inductor **206** to C_2 and the load.

[0007] Two common methods of operating DC-to-DC converter circuit **20** are in either continuous mode or discontinuous mode. If the current through the inductor **206** never falls to zero during a commutation cycle (i.e. the time period to perform both the on-state and the off-state), DC-to-DC converter circuit **20** is said to operate in continuous mode and typically the on-state operates for a shorter

period of time when compared to the off-state. Discontinuous mode of operation for DC to DC converter circuit **20** occurs when the amount of energy required by the load is small enough to be transferred in a time period smaller than the whole commutation cycle. Typically, the current through inductor **206** falls to zero for a short time period after the off-state period and therefore inductor **206** is completely discharged at the end of the commutation cycle. The commutation cycle therefore includes the on-state, the off-state and the short time period during which the inductor current is zero.

[0008] A conventional “resonant” method for achieving virtually zero power loss when switching a switch is to apply a direct current voltage input voltage V_{in} across a switch (with a diode connected across the switch, the diode is reverse biased with respect to V_{in}) in series with an inductor L and a capacitor C. The output voltage of the circuit is derived across the capacitor. The output voltage of the circuit could then in principle be connected to the input of a power converter, for example a buck-loaded series tank circuit with load. The resonant frequency of the series inductor L and capacitor C is given by Eq. 1 and the corresponding resonant periodic time T given in Eq. 2.

$$f_o = 1/2\pi(LC)^{1/2} \quad \text{Eq.1}$$

$$T = 1/f_o \quad \text{Eq.2}$$

A pulse response of the circuit means that when the switch turns on, there is both zero current in the inductor and zero voltage across the capacitor (Power=Volts X Current=0x0=zero power loss at turn on). During steady state operation of the circuit, the inductor current and capacitor voltage are sinusoidal and have a 90 degrees phase shift with respect to each other. When the switch turns off (the on period of the switch corresponds to half of the resonant periodic time) there is zero current in the inductor and maximum positive voltage (i.e. $V_{capacitor}=V_{in}$) across the capacitor (Power=Volts X Current= V_{in} x0=zero power loss at turn off).

BRIEF SUMMARY

[0009] According to an embodiment of the present invention there is provided a method for providing non-resonant zero-voltage switching in a switching power converter. The switching power converter converts power from input power to output power during multiple periodic switching cycles. The switching power converter includes a main switch and an auxiliary capacitor adapted for connecting to the main switch, and an inductor connectible to the auxiliary capacitor. When the main switch is on, a previously charged (or previously discharged) auxiliary capacitor is connected to the main switch with auxiliary switches. The main switch is switched off with zero voltage while discharging non-resonantly (charging) the auxiliary capacitor by providing a current path to the inductor. The auxiliary capacitor is disconnected from the main switch. The voltage of the auxiliary capacitor is charged and discharged alternatively during subsequent switching cycles. The voltage of the auxiliary capacitor stays substantially the same until the subsequent turn off of the main switch during the next switching cycle with substantially no energy loss in the auxiliary capacitor. The switch may include a: silicon controlled rectifier (SCR), insulated gate bipolar junction transistor (IGBT), bipolar junction transistor (BJT), field effect transistor (FET), junction field effect transistor (JFET),

switching diode, electrical relay, reed relay, solid state relay, insulated gate field effect transistor (IGFET), diode for alternating current (DIAC), and/or triode for alternating current TRIAC.

[0010] According to the present invention there is provided a switching converter including a buck stage and/or a boost stage including a main switch connecting an input voltage terminal to a first node; an auxiliary capacitor adapted for connecting to the main switch and an inductor adapted for connecting to the first node. The first node is connectible to the auxiliary capacitor by at least two current paths. When the main switch is on, a previously charged (or previously discharged) auxiliary capacitor is connected across the main switch typically with auxiliary switches. The main switch is switched off with zero voltage while discharging (charging) the auxiliary capacitor by providing a current path to the inductor. The auxiliary capacitor is disconnected from the switch. The voltage of the auxiliary capacitor is charged and discharged alternatively during subsequent switching cycles. The voltage of the auxiliary capacitor stays substantially the same until the subsequent turn off of the main switch during the next switching cycle with substantially no energy loss in the auxiliary capacitor. The switching converter may include a single buck stage or a single boost stage.

[0011] According to the present invention there is provided a switching converter included a plurality of main switches interconnected in a full bridge topology, the main switches including a first switch, a second switch, a third switch and a fourth switch. A pair of input voltage terminals are attachable at a first node connecting the first and third switches and at a second node connecting the second and fourth switches. A first output voltage terminal is operatively attached at a third node connecting the third and fourth switches. A second output voltage terminal is operatively attached at a fourth node connecting the first and second switches. Bidirectional switches are interconnected in a full bridge topology. The bidirectional switches include a first bidirectional switch, a second bidirectional switch, a third bidirectional switch and a fourth bidirectional switch. The third node connects the first and third bidirectional switches and the fourth node connects the second and fourth bidirectional switches. An auxiliary capacitor connects at one end at a node connecting the first and second bidirectional switches and at the other end at a node connecting the second and fourth bidirectional switches. The main switches are preferably configured to be periodically switched on and off during a plurality of switching cycles. One or more of the main switches is on. A previously charged (or previously discharged) auxiliary capacitor is connected across the main switch typically with auxiliary switches. The main switch is switched off with zero voltage while discharging (charging) the auxiliary capacitor by providing a current path to the inductor. The auxiliary capacitor is disconnected from the switch. The voltage of the auxiliary capacitor is charged and discharged alternatively during subsequent switching cycles. The voltage of the auxiliary capacitor stays substantially the same until the subsequent turn off of the main switch during the next switching cycle with substantially no energy loss in the auxiliary capacitor. A first inductor is typically attachable between the first output voltage terminal and the third node. A second inductor is typically attachable between the second output voltage terminal and the fourth node. The first and second inductor is optionally a single split inductor or

inductor is a single inductor connected in series to a transformer primary or other circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention is herein described, by way of example only, with reference to the accompanying drawings, wherein:

[0013] FIG. 1 shows a typical conventional buck-boost DC-to-DC converter circuit.

[0014] FIG. 2a illustrates the buck phase or on-state circuit of conventional DC-to-DC converter circuit.

[0015] FIG. 2b illustrates the boost phase or off-state circuit of DC-to-DC converter circuit 20;

[0016] FIG. 3 (FIGS. 3a-3d) illustrate a buck-boost DC-to-DC converter, according to an embodiment of the present invention;

[0017] FIG. 4 shows a flow diagram of a method for zero voltage switching, running in either continuous or discontinuous mode during the turn off of main switches Q_1 and/or Q_3 , according to embodiments of the present invention;

[0018] FIG. 5 shows another embodiment of present invention as applied to a full bridge switched DC-to-DC converter.

[0019] FIG. 6 shows a timing diagram of selected voltages and currents in the embodiment of FIG. 5.

[0020] The foregoing and/or other aspects will become apparent from the following detailed description when considered in conjunction with the accompanying drawing figures.

DETAILED DESCRIPTION

[0021] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain the present invention by referring to the figures.

[0022] It should be noted, that although the discussion herein relates to buck, boost, buck-boost full bridge switching topologies, the present invention may, by non-limiting example, alternatively be configured as well using other types of switching power DC-DC converters including half bridge, flyback, Cuk, as well as DC-AC inverters for both power supply and regulation applications.

[0023] Before explaining embodiments of the invention in detail, it is to be understood that the invention is not limited in its application to the details of design and the arrangement of the components set forth in the following description or illustrated in the drawings. The invention is capable of other embodiments or of being practiced or carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein is for the purpose of description and should not be regarded as limiting.

[0024] The term “switch” as used herein refers to any type of switch known in the art of electronics switches such as silicon controlled rectifier (SCR), insulated gate bipolar junction transistor (IGBT), bipolar junction transistor (BJT), field effect transistor (FET), junction field effect transistor (JFET), switching diode, electrical relay, reed relay, solid state relay, insulated gate field effect transistor (IGFET), DIAC, and TRIAC.

[0025] The term “zero voltage switching” (or “ZVS”) as used herein is that the peak voltage across a switch, is reduced to substantially zero volts when the switch is being turned either on or off.

[0026] The term “cycle” or “commutation cycle” refers to the periodicity of main switch positions in a circuit which performs a process of electrical power conversion or inversion.

[0027] The term “power converter” as used herein applies to DC-to-DC converters, AC-to-DC converters, DC-to-AC inverters, buck converters, boost converters, buck-boost converters, buck/boost converters, full-bridge converters and half-bridge converters or any other type of electrical power conversion/inversion known in the art.

[0028] The term “buck-boost” converter as used herein refers to a buck converter followed by a boost converter.

[0029] The term “non-resonant” as used herein to exclude resonant and quasi-resonant circuits and methods as are known in the prior art for achieving zero voltage switching.

[0030] The terms “charging” and “discharging” in the context of the present invention in reference to charging and discharging a capacitor, are used herein interchangeably except that current flow while charging and discharging is usually in the opposite direction.

[0031] Reference is now made to FIG. 3 (FIGS. 3a-3d) showing a buck-boost DC-to-DC converter 40 according to an embodiment of the present invention. A buck circuit 42 of buck-boost DC-to-DC converter 40 has an input voltage V_{in} with an input capacitor C_1 connected in parallel across V_{in} . Two switches Q_1 and Q_2 are connected in series at node A by connecting the source of Q_1 to the drain of Q_2 . The drain of Q_1 and the source of Q_2 are placed in parallel across capacitor C_1 . A zero-voltage switching feature according to embodiments of the present invention is provided using components: switches Q_{bu} , Q_{abu} , auxiliary (AUX) capacitor C_{bu} and diodes D_{2bu} and D_{abu} in buck circuit 42. The cathode of diode D_{2bu} is connected to one end of capacitor C_{bu} . The other end of C_{bu} is connected to the drain of switch Q_{bu} . The drain of Q_{abu} and the anode of diode D_{2bu} are connected in parallel across capacitor C_1 . The cathode of diode D_{abu} is connected to the source of switch Q_{bu} . The anode of diode D_{abu} and the source of switch Q_{abu} are connected across with capacitor C_{bu} . Node A shared by the cathode of diode D_{abu} and the source of switch Q_{bu} is connected to the buck end of inductor 206.

[0032] The other end of inductor 206 is connected to a boost circuit 44 of buck boost DC-to-DC converter 40 at node B. Two switches Q_4 and Q_3 are connected in series. The source of Q_4 connects to the drain of Q_3 at node B. The drain of Q_4 and the source of Q_3 connect across capacitor C_2 , across capacitor C_2 is the output voltage V_{out} of buck-boost DC-to-DC converter 40. Additional components: switches Q_{bo} , Q_{abo} , auxiliary (AUX) capacitor C_{bo} , and diodes D_{1bo} , D_{abo} are added to achieve zero-voltage switching in boost circuit 44. The anode of diode D_{1bo} is connected to one end of capacitor C_{bo} . The other end of C_{bo} is connected to the source of switch Q_{bo} and the drain of Q_{abo} . The source of Q_{abo} and the cathode of diode D_{1bo} are connected in parallel across capacitor C_2 . The anode of diode D_{abo} is connected to the drain of switch Q_{bo} . The node between the anode of diode D_{abo} and the drain of switch Q_3 are connected to node B. The cathode of diode D_{abo} and the source of switch Q_{bo} are connected across with capacitor C_{bo} .

[0033] Reference is still made to buck-boost DC-to-DC converter 40 shown in FIGS. 3a-3d which illustrate operation of buck-boost DC-to-DC converter 40. Reference is now also made to FIG. 4 showing a flow diagram of a method for zero voltage switching, in boost and/or buck topologies during the turn off of main switches Q_1 and/or Q_3 , according to embodiments of the present invention.

[0034] Step A. Before switching phase: In FIG. 3a, current flow in buck circuit 42 and boost circuit 44 is indicated by arrow markings and gray shaded line. In buck circuit 42, switch Q_1 is on (step 400), switch Q_2 is off and switch Q_{bu} is on. Auxiliary (AUX) capacitor C_{bu} is previously charged to V_{in} and connected to the source of Q_1 (step 402). I_L current flows from input, through Q_1 through node A to inductor 206.

[0035] Meanwhile, in boost circuit, Q_3 is on, Q_4 is off, Q_{bo} is on. C_{bo} is previously charged to V_{out} . I_L current flows from inductor 206 through node B.

[0036] Step B. Switching off phase: In FIG. 3b, current flow in buck circuit 42 and boost circuit 44 is indicated by the arrow markings and gray shaded lines. Switch Q_1 turns off at substantially zero voltage (step 404). Switch Q_{bu} is still on. I_L current (of inductor 206) discharges capacitor C_{bu} to zero voltage through node A through diode D_{2bu} . Q_2 turns on and Q_{bu} turns off disconnecting (step 406) auxiliary (AUX) capacitor C_{bu} .

[0037] Meanwhile, in boost circuit 44 Q_3 turns off at substantially zero voltage. I_L current (of inductor 206) discharges capacitor C_{bo} to zero voltage through node B through diode D_{1bo} . Q_4 turns on and Q_{bo} turns off disconnecting auxiliary (AUX) capacitor C_{bo} .

[0038] Thus ends one switching cycle. Now, for the next switching cycle:

[0039] Step C. Before switching phase: In FIG. 3c current flow in buck circuit 42 and boost circuit 44 is indicated by the arrow markings and Grey shaded line. Switch Q_1 is on, Switch Q_2 is off (step 400). Switch Q_{abu} turns on. C_{bu} remains discharged from the previous switching cycle and still connected to the source of Q_1 (step 402). I_L current flows from input through node A, through Q_1 to inductor 206.

[0040] Meanwhile in boost circuit 44: Q_3 is on, Q_4 is off, Q_{abo} turns on. C_{bo} remains discharged from the previous switching cycle.

[0041] Step D. Switching off phase: In FIG. 3d, current flow in buck circuit 42 and boost circuit 44 is indicated by the arrow markings and Grey shaded line. Switch Q_1 turns off with substantially zero voltage (step 404). Switch Q_{bu} is still on. I_L current (of inductor 206) charges capacitor C_{bu} to V_{in} voltage through node A through diode D_{abu} . Switch Q_2 turns on. Q_{abu} is turned off and auxiliary (AUX) capacitor C_{bu} disconnected from the source of Q_1 (step 406).

[0042] Meanwhile in the boost circuit 44, Q_3 turns off at substantially zero voltage. I_L current (of inductor 206) charges capacitor C_{bo} to V_{out} voltage through node B through diode D_{abo} . Q_4 turns on and Q_{abo} turns off.

[0043] Thus ends the second switching cycle. Now, for the next switching cycle the sequence starts again at Step A.

[0044] FIG. 5 shows a further embodiment of present invention as applied to a full bridge DC to DC converter 50. Full bridge DC to DC converter 50 has four main switches $S_{m,1}$, $S_{m,2}$, $S_{m,3}$ and $S_{m,4}$ connected together in a full bridge configuration. Each of the four main switches ($S_{m,1}$, $S_{m,2}$, $S_{m,3}$ and $S_{m,4}$) have respective diode shunts connected in parallel thereto. The diodes placed across switches $S_{m,1}$ and

$S_{m,2}$ are in both the same direction similarly the diodes of $S_{m,3}$ and $S_{m,4}$ are both in the same direction. All diodes connected across switches $S_{m,1}$, $S_{m,2}$, $S_{m,3}$ and $S_{m,4}$ are reverse biased with respect to the input voltage V_{in} . An input voltage (V_{in}^-) of full bridge DC-to-DC converter **50** is connected across the node between switches $S_{m,2}$ and $S_{m,4}$ and an input voltage (V_{in}^+) is connected at the node between switches $S_{m,1}$, and $S_{m,3}$. An output voltage (V_{out}^-) of full bridge DC-to-DC converter **50** is connected across the node between switches $S_{m,1}$ and $S_{m,2}$ connected through a split inductor **500a** and output voltage V_{out}^+ is connected at the node between switches $S_{m,3}$ and $S_{m,4}$ through a split inductor **500b**. A bi-directional switch unit **502** includes four bidirectional switches. Each bidirectional switch includes has two switches in series, e.g. ($S_{a,1}$, $S_{a,2}$) each with a diode connected across each switch with the diodes connected in opposite directions. Bi-directional switch unit **502** is connected at X1 to the node between switches $S_{m,1}$ and $S_{m,2}$ and at X2 to the node between switches $S_{m,3}$ and $S_{m,4}$. Bidirectional auxiliary switches are formed between nodes Y1 and X1 using switches $S_{a,1}$ and $S_{a,2}$, between nodes Y1 and X2 using switches $S_{a,5}$ and $S_{a,6}$, between nodes Y2 and X1 using switches $S_{a,3}$ and $S_{a,4}$ and between nodes Y2 and X2 using switches $S_{a,7}$ and $S_{a,8}$. An auxiliary capacitor C_{aux} is connected between nodes Y1 and Y2.

[0045] In different embodiments the present invention may be configured to operate in either continuous or discontinuous current mode. The operation of full bridge circuit **50**, according to a feature of the present invention and with reference again to FIG. 5 and FIG. 6 which shows a timing diagram of selected voltages and currents for steps A to H is as follows:

[0046] A) Switches $S_{m,2}$, $S_{m,3}$, $S_{a,3}$, $S_{m,4}$, $S_{m,5}$, and $S_{a,6}$ are turned on, all other switches are off. Current flows from V_{out}^- to V_{in}^- through inductor **500a**, and through main switch $S_{m,2}$. Current flows from V_{in}^+ to V_{out}^+ through $S_{m,3}$ and through inductor **500b**. Capacitor C_{aux} is charged so that node Y1 approaches V_{in}^+ and node Y2 approaches V_{in}^- .

[0047] B) $S_{m,2}$ and $S_{m,3}$ are switched open (off). Switches $S_{a,3}$, $S_{m,4}$, $S_{a,5}$, and $S_{a,6}$ remain on. During the switching open of $S_{m,2}$ and $S_{m,3}$ current from inductor **500a** and **500b** is diverted respectively through bidirectional switches ($S_{a,3}$, $S_{a,4}$) and ($S_{a,5}$, $S_{a,6}$) with voltage across switches $S_{m,2}$ and $S_{m,3}$ substantially zero. All inductor current flows through C_{aux} from node Y2 to node Y1 which during a period of time dependent on the current in inductors **500a** and **500b** and the capacitance of C_{aux} inverts the voltage across C_{aux} so that node Y1 is charged to a voltage level equal to V_{in}^- and node Y2 is charged to a voltage level equal to V_{in}^+ via auxiliary capacitor C_{aux} .

[0048] C and D) Once C_{aux} is fully charged and inverted, node Y1 is charged to V_{in}^- and Y2 is charged to V_{in}^+ , current now flows from V_{out}^- through inductor **500a** through parallel connected diode of $S_{m,1}$ and current flows from V_{in}^- through the parallel connected diode of $S_{m,4}$ and through inductor **500b** to V_{out}^+ .

[0049] E) Auxiliary switches $S_{a,3}$, $S_{a,4}$, $S_{a,5}$, and $S_{a,6}$ are now turned off with no current flowing through them nor a voltage across them.

[0050] F) Main switches $S_{m,1}$ and $S_{m,4}$ are turned on with substantially zero voltage across them, diverting most of the current from flowing through their parallel connected diodes to flowing through switches $S_{m,1}$ and $S_{m,4}$ themselves.

[0051] G) Before the turn on of $S_{m,2}$ and $S_{m,3}$, main switches $S_{m,1}$ and $S_{m,4}$ are turned off with zero voltage across them so that current flow is diverted again through their parallel connected diodes.

[0052] H) Main switches $S_{m,2}$ and $S_{m,3}$ turn on to begin the next switching cycle. Current of inductor **500a** flows from V_{out}^- through inductor **500a**, through switch $S_{m,2}$ to V_{in}^- ; and current of inductor **500b** flows from V_{in}^+ through $S_{m,3}$ to V_{out}^+ .

[0053] I) Auxiliary switches $S_{a,1}$, $S_{a,2}$, $S_{a,7}$ and $S_{a,8}$ are turned on with zero voltage and zero current.

[0054] J) $S_{m,2}$ and $S_{m,3}$ open at zero voltage. All inductor current flows now through from V_{out}^- through inductor **500a**, through bidirectional switch ($S_{a,1}$, $S_{a,2}$), through C_{aux} , through bidirectional switch ($S_{a,1}$, $S_{a,2}$) from node Y1 to node Y2 which over a period of time (dependent on the current in inductors **500a** and **500b** and the capacitance of C_{aux}) inverts again the voltage across C_{aux} so that node Y1 is charged to a voltage level equal to V_{in}^+ and node Y2 is charged to a voltage level equal to V_{in}^- (as it was in (1)).

[0055] K) Current flows from V_{out}^- through inductor **500a**, through the parallel connected diode of $S_{m,1}$ to V_{in}^+ . Current flows from V_{in}^- through the parallel connected diode of $S_{m,4}$ and through inductor **500b** to V_{out}^- .

[0056] L) Auxiliary switches $S_{a,1}$, $S_{a,2}$, $S_{a,7}$, and $S_{a,8}$ are turned off with zero voltage and zero current.

[0057] M) Main switches $S_{m,1}$ and $S_{m,4}$ are turned on at zero voltage forcing the current through themselves from V_{out}^- through inductor **500a**, through $S_{m,1}$, and from V_{in}^- through $S_{m,4}$ and through inductor **500b** to V_{out}^+ .

[0058] N) Before $S_{m,2}$ and $S_{m,3}$ are turned on, main switches $S_{m,1}$ and $S_{m,4}$ are turned off with zero voltage, the current flowing again from V_{out}^- through inductor **500a**, through the diode of $S_{m,1}$, through V_{in}^+ and from V_{in}^- through the diode of $S_{m,4}$ and through inductor **500b** to V_{out}^+ .

[0059] O) Main switches $S_{m,2}$ and $S_{m,3}$ turn on to begin the next switching cycle. The current flows again from V_{out}^- through inductor **500a**, through $S_{m,2}$ to V_{in}^- and from V_{in}^+ , through $S_{m,3}$ and through inductor **500b** to V_{out}^+ .

[0060] P) $S_{a,3}$, $S_{a,4}$, $S_{a,5}$, and $S_{a,6}$ are turned on with zero voltage and zero current.

[0061] During the two switching cycles as shown, auxiliary capacitor C_{aux} is charged and discharged by the inductor current with substantially no energy loss due to switching.

[0062] The definite articles “a”, “an” is used herein, such as “a converter”, “a switch” have the meaning of “one or more” that is “one or more converters” or “one or more switches”.

[0063] Although selected embodiments of the present invention have been shown and described, it is to be understood the present invention is not limited to the described embodiments. Instead, it is to be appreciated that changes may be made to these embodiments without depart-

ing from the principles and spirit of the invention, the scope of which is defined by the claims and the equivalents thereof.

1-9. (canceled)

10. A method comprising:

charging, through a first switch, a capacitor during a first switching cycle when the first switch is closed at a first time;

discharging the capacitor to an output terminal through an inductor connected between a first node and the output terminal when the first switch is open; and

charging, through a second switch, the capacitor during a second switching cycle when the second switch is closed at a second time.

11. The method of claim 10, further comprising:

discharging the capacitor to the output terminal when the second switch is off.

12. The method of claim 10, wherein discharging the capacitor further comprises discharging the capacitor to an additional output terminal through an additional inductor connected between a second node and the additional output terminal.

13. The method of claim 12, wherein the inductor and the additional inductor are connected in series.

14. The method of claim 10, wherein connecting the capacitor across the first switch comprises connecting the capacitor using a bidirectional switch unit.

15. The method of claim 14, wherein the bidirectional switch unit comprises a plurality of bidirectional switches arranged in a full bridge topology.

16. The method of claim 15, one or more of the plurality of bidirectional switches comprises first and second switch-diode pairs arranged in series.

17. The method of claim 16, wherein diodes in the first and second switch-diode pairs are connected in opposite directions.

18. The method of claim 10, further comprising charging the capacitor with current from the inductor during one or more switching cycles.

19. The method of claim 18, wherein charging the capacitor with current from the inductor comprises inverting a voltage across the capacitor.

20. A method comprising:

charging a capacitor through a first switch of a plurality of main switches;

diverting current from an inductor to the capacitor through at least one bidirectional switch of a plurality of bidirectional switches while the first switch is off; inverting a charge on the capacitor; and charging the capacitor across through a second switch of the plurality of main switches.

21. The method of claim 20, wherein the plurality of main switches are arranged in a full bridge topology.

22. The method of claim 20, wherein the plurality of bidirectional switches are arranged in a full bridge topology.

23. The method of claim 20, further comprising:

diverting current from the inductor to the capacitor through a different bidirectional switch from the at least one bidirectional switch when the second switch while the second switch is off.

24. The method of claim 20, wherein a voltage across the first switch is substantially zero while the current is diverted from the inductor to the capacitor.

25. A method comprising:

connecting a first terminal of a capacitor to a first voltage source via a first main switch of a plurality of main switches and a first bidirectional switch of a plurality of bidirectional switches;

connecting a second terminal of a capacitor to a second voltage source via a second main switch of the plurality of main switches and a second bidirectional switch of the plurality of bidirectional switches;

disconnecting the first and second terminals from the first and second voltage sources by turning the first and second main switches off;

diverting current from a first inductor to the first terminal via the first bidirectional switch; and

diverting current from a second inductor to the second terminal via the second bidirectional switch.

26. The method of claim 25, further comprising inverting a charge on the capacitor.

27. The method of claim 25, wherein the first voltage source is a positive voltage source and the second voltage source is a negative voltage source.

28. The method of claim 25, wherein the voltages across the first and second main switches is substantially zero when the current is diverted from the first and second inductors.

29. The method of claim 25, wherein the first and second inductors are connected in series.

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